Service d'électronique et de microélectronique

Propositions de sujets 2014-15

Proposals

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1. SEMI_CROBOT_OV : Conception et réalisation de balises de localisation pour la coupe de robotique

CONTEXT/KEYWORDS : L'objectif est de concevoir et de réaliser un dispositif électronique permettant de mesurer la distance entre deux balises, en s'affranchissant autant que possible des perturbations extérieures (électromagnétiques, ultrasoniques, ...). Un tel système permettrait à un robot

- de savoir où se trouve le robot adverse afin d'éviter de le percuter.
- de savoir où il se trouve sur la table si on connaît la distance par rapport à 3 balises fixes.

Une localisation angulaire de la balise est un atout supplémentaire. Ceci sous-entend que plusieurs balises doivent fonctionner en même temps, ce qui implique de discriminer les balises..

OBJECTIFS:

- concevoir une technologie susceptible de localiser des balises fixes et mobiles
- calculer en temps réel la distance et la position
- éviter des obstacles
- rendre le système robuste et insensible aux interférences
- localiser la position sur un espace 2D avec l'information de distance et angle (par rapport aux autres balises)

REQUIRED/DESIRED SKILLS: C/Java

NOMBRE D'ETUDIANTS : 1

PROMOTEUR(S) :

- C. Valderrama (P) UMons - Service d'électronique – 31 Bd Dolez, 7000 Mons
- Olivier Verlinden (CP) UMons Service de Mécanique rationnelle, Dynamique et Vibrations

2. SEMi_ROCCC_Vivado_CV: Evaluating synthesis techniques for Hardware implementation of sequential programs on FPGAs

CONTEXTE/KEYWORDS: The use of FPGAs in the last decade have proven the reliability and performance of such systems in the domain of processing power and speeding up software applications. However, FPGA designs need a considerable amount of time for implementation and testing. Due to the long time-to-market problem when using FPGAs, researchers and companies are seeking tools that can shorten this time. In this context, several tools have been developed that can automatically migrate sequential codes (C/C++) into hardware description languages codes suitable for implementing on FPGAs. In this project, the student is required to explore these tools, specifically ROCCC, CatapultC and Vivado, and compare their performance and reliability.

Keywords: High level synthesis, parallel programming, hardware synthesis, FPGA, compilers, C programming

OBJECTIFS: The project consists of:

- A review of the tool ROCCC established in the University of California Riverside (UCR) and available from Jacquard Computing Inc.
- A similar review and understanding of the Vivado(Xilinx) and CatapultC(Mentor) EDA tools.
- Study the possibility to migrate a sequential C program into FPGAs by combining both the ROCCC, Vivado and CatapultC compilers and exploring the most beneficial technique used. Benefits are in terms of speed, reliability, hardware resources and functionality.
- Develop an automatic scripting code calling any of ROCCC, Vivado, and CatapultC in order to automatically allow the user to see the results.

TASKS: The following tasks must be accomplished:

- Periodical presentations and activity reports are mandatory in order to track the progress of the work.
- A full system correct functionality using the ROCCC compiler. A test sample must be given and the student should show how the system works and how to test the reliability of the compiler's output.
- A full system correct functionality using the Vivado and CatapultC compilers. A test sample must be given and the student should show how the system works and how to test the reliability of the compiler's output.
- Develop a system taking a sequential C code, call ROCCC, Vivado and CatapultC and finally producing an HDL code that will be implemented on an FPGA.
- Study and analysis of the full system performance, comparing ROCCC, Vivado and CatapultC and highlight the advantages of these techniques. Results in execution times, power, energy, time-to-market and similar issues should be addressed in the final report of the student.
- A final report discussing the achievements done in the project.

REQUIRED/DESIRED SKILLS: C/C++ programming, HDL programming (VHDL or Verilog), OS (Windows, MAC OS; advantage), Good presentation skills (both report wise and oral presentation wise), Good English skills.

REFERENCES: the following references will be provided: …
NOMBRE D'ETUDIANTS : 1

PROMOTEUR : C. Valderrama (P)

3. SEMI_DNA1_XC1: Implementation of Sequence Alignment Algorithm on FPGA using HLS tools

CONTEXTE/KEYWORDS: Bioinformatics focuses on developing computational methods for collecting, handling and analyzing biological data leading to the discovery and fundamental understanding of the genetic composition in organisms. The bioinformatics community faces a daunting challenge today because the rate of data generation is rapidly outpacing the rate at which it can be computationally processed. A special area of study in bioinformatics is sequence alignment, which analyzes similarities between DNA or protein sequences to assess the genetic relationship between organisms or species. The sequence similarity may also be the consequence of structural or functional relationships. Sequence alignment has all the typical characteristics of a bioinformatics application such as large data amount, small data size and low data interdependence. Thus, finding a strategy to accelerate the sequence alignment algorithm can provide a good reference for the other applications in bioinformatics fields.

High-level synthesis (HLS) sometimes also referred as C synthesis, electronic system-level synthesis. It is an automated design process that interprets an algorithmic description of a desired behavior and creates digital hardware that implements that behavior. The goal of HLS is to let hardware designers efficiently build and

verify hardware, by giving them better control over optimization of their design architecture, and through the nature of allowing the designer to describe the design at a higher level of tools while the tool does the RTL implementation. Verification of the RTL is an important part of the process.

OBJECTIFS: The aims of this project are to learn the FPGA development flow, understand the principles of sequence alignment algorithms and finally implement one sequence alignment algorithm on FPGA by using HLS tool (Vivado).

TACHES :

1. Get familiar with DNA sequence alignment algorithms and selected one sequence alignment algorithm.
2. Get familiar with FPGA development and HLS tool (Vivado HLS).
3. Create the C code for the selected sequence alignment algorithm.
4. High level synthesis the C project.
5. Implement the project on FPGA.

REQUIRED/DESIRED SKILLS: C++ Programming ; FPGA development; Vivado; Skill of HDL language is preferred.

REFERENCES:

Wiki page of Sequence Alignment Algorithms: http://en.wikipedia.org/wiki/Sequence_alignment

Vivado HLS: http://www.xilinx.com/products/design-tools/vivado/integration/esl-design/

NOMBRE D'ETUDIANTS : 1
PROMOTEUR : C. Valderrama (P), Xin Chang (CP)

4. SEMI_DPR_FE1: FPGA Implementation of a simple algorithm supporting Partial Dynamic Reconfiguration (DPR)

CONTEXTE/KEYWORDS: One of the most powerful abilities of current FPGAs is their ability for self-reconfiguration in runtime, with or without user interaction. Their versatility and low power consumption makes them perfect for architectural exploration of parallel applications at low cost. In order to integrate these abilities into current developments it's necessary to better study their implementation, programming models, requirements and limitations

OBJECTIFS: The project's goal is to implement an algorithm's architecture on the FPGA, employing DPR. Different programming and reconfiguration strategies are to be evaluated to establish the pros and cons of each one. Simple functions and hardware blocks will be first considered to learn the basics of DPR, after that, a more complex algorithm will be implemented.

TACHES:

6. Get familiar with DPR basics.
7. Develop a simple project employing DPR
8. Study suitable algorithms for hardware implementation
9. Implement the selected algorithm in hardware using DPR

REQUIRED/DESIRED SKILLS: Matlab; VHDL or Verilog; C/C++ programming; Basic knowledge of FPGA.

REFERENCES: reading material will be provided including source code and recent published algorithm

NOMBRE D'ETUDIANTS : 1
PROMOTEUR : C. Valderrama (P), Fernando Escobar (CP)

5. SEMI_B&BModel_FE2: Performance Modeling of a Branch-and-Bound Optimization Algorithm in an Embedded Platform

CONTEXTE/KEYWORDS: Nowadays, the number of processor cores in computers keeps going up to enhance their computational power. Multicore and specialized processors like GPUs are currently suffering from memory access bottlenecks produced by irregular and data dependent accesses. Optional processing platforms like FPGAs and SoCs (Multicore + FPGA) are systems that can help overcome such limitations due to their versatility.

OBJECTIFS/TACHES:

- Getting familiar with a simple Branch N Bound algorithm.
- Implementing and profiling the algorithm in MATLAB and C++
- Getting familiar with FPGAs
- Implementing the algorithm in an FPGA based platform.
- Analyze performance bottlenecks and propose an optimization solution.
- Implement a Hardware/Software solution.

REQUIRED/DESIRED SKILLS: we prefer students who are interested in combined software-hardware solutions, have a background in FPGA and/or C programming and have a strong sense of responsibility and independence.

REFERENCES: References provided during project development.

NOMBRE D'ETUDIANTS: 1

PROMOTEURS: C. Valderrama (P SEMI), F. Escobar (CP SEMI)

6. SEMI_DPModel_FE3: Performance Modeling of a Dynamic Programming Optimization Algorithm in an Embedded Platform

CONTEXTE/KEYWORDS: Nowadays, the number of processor cores in computers keeps going up to enhance their computational power. Multicore and specialized processors like GPUs are currently suffering from memory access bottlenecks produced by irregular and data dependent accesses. Optional processing platforms like FPGAs and SoCs (Multicore + FPGA) are systems that can help overcome such limitations due to their versatility.

OBJECTIFS/TACHES: Getting familiar with a simple Dynamic Programming algorithm. Implementing and profiling the algorithm in MATLAB and C++; Getting familiar with FPGAs; Implementing the algorithm in an FPGA based platform. Analyze performance bottlenecks and propose an optimization solution. Implement a Hardware/Software solution.

REQUIRED/DESIRED SKILLS: we prefer students who are interested in combined software-hardware solutions, have a background in FPGA and/or C programming and have a strong sense of responsibility and independence.

REFERENCES: References provided during project development.

NOMBRE D'ETUDIANTS: 1

PROMOTEURS: C. Valderrama (P SEMI), F. Escobar (CP SEMI)

7. SEMi_NOCA_LJ: Analyse de solutions Network on Chip pour des applications massivement parallèles

CONTEXTE/ KEYWORDS : L'électronique est une science qui n'arrête pas d'évoluer ! Les nouveaux enjeux dans le domaine visent à pouvoir connecter facilement un grand nombre de périphériques (processeurs, mémoires, …) pour obtenir des solutions et des applications de plus en plus complexes. L'utilisation de l'architecture Network on Chip (NoC) est une alternative qui permet de résoudre ce problème. Le but de ce travail de fin d'études est de réaliser différents « testbench » afin d'analyser et comparer diverses variantes de solution Network on Chip dont la solution « Minimalist NoC » qui est une nouvelle solution mise au point dans le service. Ce sujet de TFE est le complément d'une thèse de doctorat. La possibilité de contribuer à une publication n'est donc pas exclue.

OBJECTIFS/TACHES : réaliser différents « testbench » afin d'analyser et comparer diverses variantes de solution Network on Chip dont la solution « Minimalist NoC » qui est une nouvelle solution mise au point dans le service.

REQUIRED/DESIRED SKILLS: FPGA programming language, C/C++ programming;

NOMBRE D'ETUDIANTS : 1

PROMOTEUR : C. Valderrama (P), L. Jojczyk (CP)

8. SEMi_NOCR_LJ: Réalisation d'une application Network on Chip massivement parallèle sur FPGA

CONTEXTE/ KEYWORDS : La mise au point d'applications multimédias est un problème critique. En effet, ce type d'application demande généralement des contraintes de fonctionnement strictes (délai, ressources ,…). De plus, avec l'évolution des technologies, le fonctionnement en parallèle de certains traitements est un problème d'actualité. Le but de ce TFE est de mettre au point une application multimédia massivement parallèle utilisant une architecture d'interconnexion NoC. La première étape est la mise au point d'un modèle de simulation haut niveau pour réaliser l'exploration de l'espace de solution. Ensuite, une implémentation physique sur FPGA sera réalisée et sera comparée au modèle de simulation. Ce sujet de TFE est le complément d'une thèse de doctorat. La possibilité de contribuer à une publication n'est donc pas exclue.

OBJECTIFS/TACHES. Le but de ce TFE est de mettre au point une application multimédia massivement parallèle utilisant une architecture d'interconnexion NoC. La première étape est la mise au point d'un modèle de simulation haut niveau pour réaliser l'exploration de l'espace de solution. Ensuite, une implémentation physique sur FPGA sera réalisée et sera comparée au modèle de simulation.

REQUIRED/DESIRED SKILLS: Any FPGA programming language, Matlab, C/C++ programming;

NOMBRE D'ETUDIANTS : 1

PROMOTEUR : C. Valderrama (P), L. Jojczyk (CP) / Xin Chang(CP)

9. SEMi_GNSS_GL: Performance analysis of GPS and Galileo towards a Global Navigation Satellite System for nano satellites

CONTEXTE/ KEYWORDS: small satellites are developed to perform short term missions in space. The power consumption and size is the main restriction of such devices. GNSS is also required in space to provide information about position, altitude and speed. However, the speed and altitude of satellites doesn't allow the use of terrestrial civil use GNSS receivers.

OBJECTIFS: The behavior of GPS and Galileo receivers will be analyses to evaluate their performance and memory requirements. Those requirements will be considered to elaborate a combined hardware/software strategy able to provide the required power processing for real-time response and power consumption limitations. In addition, other measurement strategies, such as to combine inertial MEMS information, will also be evaluated to increase the precision of the expected results.

REQUIRED/DESIRED SKILLS: Matlab, C/C++ programming, profiling, algorithms, signal processing

NOMBRE D'ETUDIANTS : 1

PROMOTEUR: C. Valderrama (P), G. Leimos (CP)

10. SEMI_VD_CV: Auto-generation of video pipeline interconnect for FPGAs

CONTEXTE: FPGAs are highly used for video processing. They interface cameras or video sources of various formats and protocols like HDMI or LVDS. A pipeline of video processing blocks usually follows in order to correct or adjust the image properties to required application. A frame buffer or synchronizer is sometimes necessary before signals are output. Again, various output options do exist: HDMI, DVI, Component, LVDS for touchscreens, etc. Though standard IPs of most components do exist, it is still today time consuming, error prone and project specific to design such a video chain. In this project, the student will study an interconnect scheme that could be used to automate such a design task.

KEYWORDS: video processing, FPGA, high speed interconnects, hardware synthesis, language generation.

OBJECTIFS: The goal of the project is to develop a method that could be used to automatically generate a video pipeline using a simple definition syntax. The definition file could simply list the desired blocks in sequence with a set of global or block specific parameters. In order to achieve this, different ways can be considered. Partial reconfiguration and bus interconnects like AXI would be studied to know if they would be suitable and what would be the advantages and limitations. The main difficulties are: to consider all the required interconnections between the various kind of blocks to propagate the imaging data but also the parameters and other control signals necessary for the blocks to work without manual customization of the code, or manual parameter adjustments. To consider that the signals can have different formats: image size, sampling rate, chroma subsampling 4:2:2/4:4:4, RAW/RGB/YCbCr, progressive or interlaced. To consider that the output signal should be in sync with a reference external signal; this impacts the whole propagation chain and delays of the various blocks.

TASKS: The following tasks must be accomplished. The development of a first simple video pipeline with a generator as input and a video output like HDMI or DVI. The review and optional

development of some simple video blocks: chroma resampling, crop and resize, color correction matrix, video input, video output. The review and optional development of interconnection blocks like domain crossing fifos, frame buffer (DDR), high speed serial interfaces (SDI, Aurora, etc.). The study of AXI4 interconnects. The study of partial dynamic reconfiguration. The study of other potential methods for block interconnection considering the goal to automatically generate the video pipeline. Decide on an architecture and develop a simple generator that could convert a definition file into a synthesizable design based on this architecture. The outcomes would be: A description of each type of processing block and it's constraints. A manually designed video pipeline with some key processing blocks. A report of the various possible methods to achieve an automatic interconnect between the blocks, analysis of the difficulties and possible solutions. An automatic generator system to build the pipeline automatically depending on some chosen parameters like image resolution.

REQUIRED/DESIRED SKILLS: Any FPGA programming language, Matlab, C/C++ programming;

NOMBRE D'ETUDIANTS : 1

PROMOTEUR : C. Valderrama (P)

11. SEMI_INFO_HetComp : Studying FPGAs and their integration in StarPU, the unified platform for task scheduling on heterogeneous multicore architectures

CONTEXTE/KEYWORDS: Nowadays, the number of processor cores in computers keeps going up to enhance their computational power. Besides, specialized processors, like GPUs or FPGAs, are also exploited to speed-up the processing of generic computations. Many tools are developed to efficiently handle systems with multi-core processors and heterogeneous computing resources. One of them is StarPU, which provides a scheduler optimizing the computation distribution on all available cores and processors (CPU or GPU).

OBJECTIFS/TACHES:

- Getting familiar with FPGAs
- Getting familiar with StarPU
- Allowing StarPU to use FPGAs
- Evaluating the solution with an algorithm (provided buy supervisors)

REQUIRED/DESIRED SKILLS: we prefer students who are interested in combined software-hardware solutions, have a background in FPGA and/or C programming and have a strong sense of responsibility and independence.

REFERENCES: C. Augonnet, S. Thibault, R. Namyst, and P.-A. Wacrenier, *StarPU: A Unified Platform for Task Scheduling on Heterogeneous Multicore Architectures*. Concurrency and Computation: Practice and Experience, Special Issue: Euro-Par 2009, 23:187-198, February 2011.

http://runtime.bordeaux.inria.fr/StarPU/

Other references are available.

NOMBRE D'ETUDIANTS: 1

PROMOTEURS: P. Manneback (P INFO) C. Valderrama (P SEMI) S. Frémal (CP INFO) F. Escobar (CP SEMI)