RAMURA DE ȘTIINȚĂ: CALCULATOARE, TEHNOLOGIA INFORMAȚIEI ȘI INGINERIA SISTEMELOR

STANDARDE MINIMALE ȘI OBLIGATORII PENTRU CONFERIREA TITLURILOR DIDACTICE DIN ÎNVĂȚĂMÂNTUL SUPERIOR
ȘI A GRADELOR PROFESIONALE DE CERCETARE-DEZVOLTARE

Candidata: conf. dr. ing. Oana Amaricai-Boncalo

Centralizator Standarde minimale necesare si obligatorii

1. Structura activității candidatului								
Nr. Crt.	Domeniul activităților	Categorii și restricții		Subcategorii		Indicatori k_{pl}	Nr. Realizat	Punctaj
0	1	2		3		4	5	6
1	Activitatea didactică și profesională (A1)	Cărți de autor sau capitole de specialitate la edituri cu ISBN	Cărți/monografii	A 1.1.1	Internaționale	50/nr. de autori	2 capitole, 12,5/5 +50/2	8.75
				A 1.1.2	Naționale	50/nr. de autori	2 cărți, 50/1 +50/2	75
		Material didactic/Lucrări didactice publicate la edituri cu ISBN	Manuale didactice	A 1.2.1		40/nr. de autori	1 lucrare didactică, 40/2	20
							TOTAL A1	103.75
		Articole în reviste cotate ISI și lucrări în volumele unor manifestări științifice indexate ISI		A 2.1		(25+30* factor impact)/ nr. de autori	44	518.46
		Articole în reviste și lucrări în volumele unor manifestări științifice indexate în alte baze de date internaționale recunoscute		A 2.2		20/nr. de autori	19	98.55
		Proprietate intelectuală, brevete de invenție, certificate ORDA		A 2.3.1	Internaționale	35/ nr. de autori		
				A 2.3.2	Naționale (OSIM)	25/ nr. de autori		

2	Activitatea de cercetare (A2)	Granturi/proiecte de cercetare câștigate prin competiție sau contracte cu agenți economici în valoare de minimum 10000 dolari SUA echivalent încasați	Director/responsabil partener	A 2.4.1.1	Internaționale	20*ani de desfășurare	2 granturi - 4 ani	80
				A 2.4.1.2	Naționale	10*ani de desfășurare	1 grant - 2 ani	20
			Membru în echipă	A 2.4.2.1	Internaționale	4*ani de desfășurare	2 granturi - 5 ani	20
				A 2.4.2.2	Naționale	2*ani de desfășurare	2 granturi- 4 ani	8
							TOTAL A2	745.01
		Citări în cărți, reviste și volume ale unor manifestări științifice		A 3.1.1	Cărți, ISI	(8/nr. aut art. citat)*2 dacă art care citează este în Q1, Q2	44	106.9
				A 3.1.2	BDI	4/nr. aut art. citat	48	57.39
		Membru în comitetele de redacție sau comitelele științifice ale revistelor indexate ISI, chair, co-chair sau membru în comitetele de organizare ale manifestărilor științifice internaționale indexate ISI		A 3.2		10	1	10

		Membru în comitetele de redacție sau comitelele științifice ale revistelor indexate BDI, chair, co-chair sau membru în comitetele de organizare ale manifestărilor științifice internaționale indexate BDI		A 3.3		6	5	30
3	Recunoașterea și impactul activității (A3)	Premii în domeniu conferite de Academia Română, ASTR, AOSR, sau premii internaționale de prestigiu		A 3.4		15		
							TOTAL A3	204.29
						TOTAL	**A1+A2+A3**	**1053**

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Condiții minimale pentru profesor/abilitare

Candidata: conf. dr. ing. Oana Amaricai-Boncalo

Centralizator Standarde minimale necesare si obligatorii

3. Condiții minimale			
Nr. crt.	Domeniul de activitate	Profesor/abilitare	Punctaj realizat
1	Activitatea didactică/profesională (A1)	100	103.75
2	Activitatea de cercetare (A2)	600	745.01
3	Recunoașterea impactului activității (A3)	150	204.29
Total A		850	1053.05

Condiții minimale obligatorii pe subcategorii		Profesor/abilitare	Realizat
A 1.1.1 - A 1.1.2	Cărți de specialitate	1 carte	3 cărți, 2 capitole
A 2.1	Articole în reviste cotate ISI și lucrări în volumele unor manifestări științifice indexate ISI proceedings	15, din care minimum 3 în reviste cotate Q1 sau Q2	51, din care 5 în reviste Q1 sau Q2
A 2.4.1	Granturi/proiecte de cercetare câștigate prin competiție (director/responsabil partener)	2	3
A 3.1.1	Număr de citări în cărți, reviste cotate ISI și volume ale unor manifestări științifice ISI (WoS)	25	44
	Factor de impact ISI cumulat pentru publicații	10	30.967

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ȘI A GRADELOR PROFESIONALE DE CERCETARE-DEZVOLTARE

A 1 Activitatea didactică și profesională

A 1.1 Cărți de autor sau capitole de specialitate la edituri cu ISBN

A 1.1.1 Internaționale

Candidata: conf. dr. ing. Oana Amaricai-Boncalo

Centralizator Standarde minimale necesare si obligatorii

Nr. Crt	Autori	Titlul cărţii	Editura	ISBN	Anul	Număr de pagini	Număr de autori	Punctaj
1	A Amaricai, O Boncalo	Chapter: "Design Trade-Offs for FPGA Implementation of LDPC Decoders", Field Programmable Gate Arrays,	InTechOpen	ISBN 978-953-51-3207-3	2017	20	2	6.25
2	A. Amaricai, A. Dobre, O. Boncalo, A. Tanase, C. Valuch	Chapter "Using Cycle-Approximate Simulation for Bus Based Multi-Processor System-On Chip Analysis" in Applied Computational Intelligence in Engineering and Information Technology	Springer	ISBN 978-3-642-28304-8	2012	12	5	2.50
							TOTAL	8.75

A 1.1.2 Naționale

Nr. Crt	Autori	Titlul cărţii	Editura	ISBN	Anul	Număr de pagini	Număr de autori	Punctaj
1	Oana Boncalo, Alexandru Amăricăi	Proiectarea circuitelor digitale folosind Verilog HDL. Analiză şi sinteză	Editura Politehnica Timişoara	ISBN 978-606-554-331-7	2011	220	2	25.00
2	Oana Boncalo	Simulation Based Reliability Assessment of Quantum Circuits	Editura Politehnica Timişoara	ISBN 978-973-625-796-4	2008	227	1	50.00
							TOTAL	75.00

A 1.2.1 Material didactic/Lucrări didactice publicate la edituri cu ISBN: Manuale didactice

Nr. Crt	Autori	Titlul cărţii	Editura	ISBN	Anul	Număr de pagini	Număr de autori	Punctaj
1	Oana Boncalo, Alexandru Amaricai	Logica Digitala-Aplicatii	Editura Politehnica Timişoara	978-606-554-581-6	2016	110	2	20.00
							TOTAL	20.00

TOTAL A1	103.75

RAMURA DE ȘTIINȚĂ: CALCULATOARE, TEHNOLOGIA INFORMAȚIEI ȘI INGINERIA SISTEMELOR
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ȘI A GRADELOR PROFESIONALE DE CERCETARE-DEZVOLTARE

A2 Activitatea de cercetare

A 2.1 Articole în reviste cotate ISI și lucrări în volumele unor manifestări științifice indexate ISI

Candidata: conf. dr. ing. Oana Amaricai-Boncalo

Centralizator Standarde minimale necesare si obligatorii

Nr. crt.	Lucrarea publicată	Nr. Autori	Impact Factor	Punctaj
1	O Boncalo, G Kolumban-Antal, A Amaricai, V Savin, D Declercq "Layered LDPC Decoders With Efficient Memory Access Scheduling and Mapping and Built-In Support for Pipeline Hazards Mitigation" IEEE Transactions on Circuits and Systems I: Regular Papers 66 (4), 2019	5	2.823	21.938
2	K Le, D Declercq, F Ghaffari, L Kessal, O Boncalo, V Savin "Variable-node-shift based architecture for probabilistic gradient descent bit flipping on QC-LDPC codes" IEEE Transactions on Circuits and Systems I: Regular Papers 65 (7),2018	6	2.823	18.28166667
3	TT Nguyen-Ly, V Savin, K Le, D Declercq, F Ghaffari, O Boncalo "Analysis and design of cost-effective, high-throughput LDPC decoders" IEEE Transactions on Very Large Scale Integration (VLSI) Systems 26 (3), 2018	6	1.744	12.88666667
4	D Declercq, V Savin, O Boncalo, F Ghaffari "An imprecise stopping criterion based on in-between layers partial syndromes" IEEE Communications Letters 22 (1), 2018	4	2.723	26.6725
5	A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4), 2010	3	2.45	32.83333333
6	A Amaricai, O Sicoe, O Boncalo "On the Redundant Representation of Partial Remainders in Radix-4 SRT Dividers" Journal of Circuits, Systems and Computers 26 (06), 2017	3	0.595	14.28333333
7	O Boncalo, G Kolumban-Antal, D Declercq, V Savin "Code-design for efficient pipelined layered LDPC decoders with bank memory organization" Microprocessors and Microsystems 63, 216-225, 2017	4	1.049	14.1175
8	O Boncalo, A Amaricai, PF Mihancea, V Savin "Memory trade-offs in layered self-corrected min-sum LDPC decoders" Analog Integrated Circuits and Signal Processing 87 (2), 2016	4	0.8	12.25
9	S Nimara, A Amaricai, O Boncalo, M Popa "Multi-Level Simulated Fault Injection for Data Dependent Reliability Analysis of RTL Circuit Descriptions" ADVANCES IN ELECTRICAL AND COMPUTER ENGINEERING 16 (1), 2016	4	0.699	11.4925
10	O Boncalo, A Amaricai, V Savin, D Declercq, F Ghaffari "Check node unit for LDPC decoders based on one-hot data representation of messages" Electronics Letters 51 (12), 2015	5	1.232	12.392
11	A Amaricai, O Boncalo, CE Gavriliu "Low-precision DSP-based floating-point multiply-add fused for Field Programmable Gate Arrays" IET Computers & Digital Techniques 8 (4), 2014	3	0.639	14.72333333
12	A Amaricai, O Boncalo "Implementation of very high radix division in FPGAs" Electronics letters 48 (18), 2012	2	1.232	30.98
13	O Boncalo, A Amăricăi, M Udrescu, M Vlăduţiu "Quantum circuit's reliability assessment with VHDL-based simulated fault injection"Microelectronics Reliability 50 (2), 2010	4	1.236	15.52

14	L Prodan, M Udrescu, O Boncalo, M Vladutiu "Design for dependability in emerging technologies" ACM Journal on Emerging Technologies in Computing Systems (JETC) 3 (2)	4	1.672	18.79
15	A. Amaricai, O. Boncalo, M. Iordate, and B. Marinescu. A Moving Window Architecture for a HW/SW Codesign Based Canny Edge Detection for FPGA. In 2012 28TH INTERNATIONAL CONFERENCE ON MICROELECTRONICS (MIEL), International Conference 2on Microelectronics-MIEL, pages 393{396. IEEE; IEEE Serbia & Montenegro Sect - ED/SSC Chapter; IEEE Electron Devices Soc (EDS); IEEE Solid-State Circuits Soc (SSCS), 2012. 28th International Conference on Microelectronics (MIEL), Nis, SERBIA, MAY 13-16, 2012	4	0.25	8.125
16	A. Amaricai, M. Vladutiu, L. Prodan, M. Udrescu, and O. Boncalo. Hardware support for combined interval and floating point multiplication. In Napieralski, A, 14th International Conference on Mixed Design of Integrated Circuits and Systems, Ciechocinek, POLAND, JUN 21-23, 2007	5	0.25	6.5
17	Alexandru Amaricai and Oana Boncalo. Improving the Performance of the Divide-Add Fused Operation Using Variable Latency Quotient Generation. In PROCEEDINGS OF THE 2009 12TH EUROMICRO CONFERENCE ON DIGITAL SYSTEM DESIGN, ARCHITECTURES, METHODS AND TOOLS, pages 45{49, 2009. 12th Euromicro Conference on Digital System Design, Architectures, Methods and Tools, Patras, GREECE, AUG 27-29, 2009	2	0.25	16.25
18	Alexandru Amaricai and Oana Boncalo. FPGA Implementation of Very High Radix Square Root with Prescaling. In 19th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2012), Seville, SPAIN, DEC 09-12, 2012	2	0.25	16.25
19	Alexandru Amaricai and Oana Boncalo. SRT Radix-2 Dividers with (5,4) Redundant Representation of Partial Remainder. In 2013 NORCHIP, Conference, Vilnius, LITHUANIA, NOV 11-12, 2013.	2	0.25	16.25
20	Alexandru Amaricai and Oana Boncalo. Cost Effective FPGA Implementation for Hard Decision LDPC Decoders. In 2016 24TH TELECOMMUNICATIONS FORUM (TELFOR), pages 246{ 249, Belgrade, SERBIA, NOV 22-23, 2016	2	0.25	16.25
21	Alexandru Amaricai, Oana Boncalo, and Ioana Mot. Memory efficient FPGA implementation for flooded LDPC decoder. In 2015 23RD TELECOMMUNICATIONS FORUM TELFOR (TELFOR), pages 500{ 503, Belgrade, SERBIA, NOV 24-26, 2015	3	0.25	10.83333333
22	Alexandru Amaricai, Oana Boncalo, Ovidiu Sicoe, and Marius Marcu. FPGA Implementation of Hybrid Fixed Point - Floating Point Multiplication. 20th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES 2013), Gdynia, POLAND, JUN 20-22, 2013.	4	0.25	8.125
23	Alexandru Amaricai, Nicoleta Cucu-Laurenciu, Oana Boncalo, Joyan Chen, Sergiu Nimara, Valentin Savin, and Sorin Cotofana. Multi-Level Probabilistic Timing Error Reliability Analysis Using a Circuit Dependent Fault Map Generation. 2015 Conference on Design of Circuits and Integrated Systems (DCIS), Estoril, PORTUGAL, NOV 25-27, 2015.	7	0.25	4.642857143
24	Alexandru Amaricai, Sergiu Nimara, Oana Boncalo, Jiaoyan Chen, and Emanuel Popovici. Probabilistic Gate Level Fault Modeling for Near and Sub-Threshold CMOS Circuits.. 7th Euromicro Conference on Digital System Design (DSD), Verona, ITALY, AUG 27-29, 2014	5	0.25	6.5

25	Alexandru Amaricai, Sergiu Nimara, Oana Boncalo, and Emanuel Popovici. Reliability analysis of memory centric LDPC decoders under probabilistic storage failures. 23rd IEEE International Conference on Electronics, Circuits and Systems (ICECS), MONACO, DEC 11-14, 2016.	4	0.25	8.125
26	Alexandru Amaricai, Valentin Savin, Oana Boncalo, Nicoleta CucuLaurenciu, Joyan Chen, and Sorin Cotofana. Timing Error Analysis of Flooded LDPC Decoders. IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS), Tel Aviv, ISRAEL, NOV 02-04, 2015.	6	0.25	5.416666667
27	Alexandru Amaricai, Mircea Vladutiu, and Oana Boncalo. Design of Floating Point Units for Interval Arithmetic. 5th International Conference on Ph D Research in MicroElectronics and Electronics, Univ Coll Cork, Cork, IRELAND, JUL 12-17, 2009	3	0.25	10.83333333
28	Alexandru Amaricai, Mircea Vladutiu, Lucian Prodan, Mihai Udrescu, and Oana Boncalo. Exploiting parallelism in double path adders' structure for increased throughput of floating point addition. 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, Lubeck, GERMANY, AUG 29-31, 2007.	5	0.25	6.5
29	Alexandru Amaricai, Mircea Vladutiu, Lucian Prodan, Nlihai Udrescu, and Oana Boncalo. Design of addition and multiplication units for high performance interval arithmetic processor. pages 223+. 10th IEEE International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Cracow, POLAND, APR 11-13, 2007.	5	0.25	6.5
30	Alexandru Amaricai, Mircea Vladutiu, Lucian Prodan, Nlihai Udrescu, and Oana Boncalo. Design of addition and multiplication units for high performance interval arithmetic processor. pages 223+, 2007. 10th IEEE International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Cracow, POLAND, APR 11-13, 2007.	5	0.25	6.5
31	Alexandru Amaricai, Mircea Vladutiu, Lucian Prodan, Nlihai Udrescu, and Oana Boncalo. Design of addition and multiplication units for high performance interval arithmetic processor. pages 223+, 2007. 10th IEEE International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Cracow, POLAND, APR 11-13, 2007.	5	0.25	6.5
32	O. Boncalo, A. Amaricai, C. Spagnol, and E. Popovici. Cost effective FPGA probabilistic fault emulation. 2014. 32nd NORCHIP Conference, Tampere, FINLAND, OCT 27-28, 2014	4	0.25	8.125
33	Oana Boncalo. QC-LDPC Gear-Like Decoder Architecture with MultiDomain Quantization. pages 244{251, 2016. 19th Euromicro Conference on Digital System Design (DSD), Limassol, CYPRUS, AUG 31-SEP 02, 2016.	1	0.25	32.5
34	Oana Boncalo and Alexandru Amaricai. Reliability Analysis of Qubit Data Movement for Distributed Quantum Computation. pages 481{487, 2009. 12th Euromicro Conference on Digital System Design, Architectures, Methods and Tools, Patras, GREECE, AUG 27-29, 2009	2	0.25	16.25
35	Oana Boncalo, Alexandru Amaricai, and Valentin Savin. Memory Efficient Implementation of Self-Corrected Min-Sum LDPC Decoder. pages 295{298, 2014. 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marseille, FRANCE, DEC 07-10, 2014	3	0.25	10.83333333

36	Oana Boncalo, Alexandru Amaricai, and Valentin Savin. Memory Efficient Implementation of Self-Corrected Min-Sum LDPC Decoder. pages 295{298, 2014. 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marseille, FRANCE, DEC 07-10, 2014	3	0.25	10.83333333
37	Oana Boncalo and Ioana Mot. Multi Clock Flooded LDPC Decoding Architecture with Reduced Memory and Interconnect. pages 697{700, 2016. IEEE-Computer-Society Annual Symposium on VLSI (ISVLSI), Pittsburgh, PA, JUL 11-13, 2016.	2	0.25	16.25
38	Oana Boncalo, Valentin Savin, and Alexandru Amaricai. Unrolled Layered Architectures For Non-Surjective Finite Alphabet Iterative Decoders. 2017. IEEE Nordic Circuits and Systems Conference (NORCAS) / NORCHIP and International Symposium of System-on-Chip (SoC), Linkoping, SWEDEN, OCT 23-25, 2017	3	0.25	10.83333333
39	Oana Boncalo, Mihai Udrescu, Lucian Prodan, Mircea Vladutiu, and Alexandru Amaricai. Assessing quantum circuits reliability with 5mutant-based simulated fault injection. pages 942{945, 2007. 18th European Conference on Circuit Theory Design, Univ Sevilla, Seville, SPAIN, AUG 26-30, 2007	5	0.25	6.5
40	Oana Boncalo, Mihai Udrescu, Lucian Prodan, Mircea Vladutiu, and Alexandru Amaricai. Saboteur-based fault injection for quantum circuits fault tolerance assessment. pages 634{640, 2007. 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, Lubeck, GERMANY, AUG 29-31, 2007	5	0.25	6.5
41	Oana Boncalo, Mihai Udrescu, Lucian Prodan, Mircea Vladutiu, and Alexandru Amaricai. Simulated fault injection for quantum circuits based on simulator commands. pages 245+, 2007. 4th International Symposium on Applied Computational Intelligence and Informatics, Timisoara, ROMANIA, MAY 17-18, 2007.	5	0.25	6.5
42	Oana Boncalo, Mihai Udrescu, Lucian Prodan, Mircea Vladutiu, and Alexandru Amaricai. Using simulated fault injection for fault tolerance assessment of quantum circuits. pages 213+, 2007. 40th Annual Simulation Symposium, Norfolk, VA, MAR 26-28, 2007.	5	0.25	6.5
43	Oana Boncalo, Mihai Udrescu, Lucian Prodan, Mircea Vladutiu, and Alexandru Amaricai. Using simulated fault injection for fault tolerance assessment of quantum circuits. pages 213+, 2007. 40th Annual Simulation Symposium, Norfolk, VA, MAR 26-28, 2007.	5	0.25	6.5
44	Andrei Hera, Oana Boncalo, Constantina-Elena Gavriliu, Alexandru Amaricai, Valentin Savin, David Declercq, and Fakhreddine Ghaffari. Analysis and Implementation of On-the-Fly Stopping Criteria for Layered QC LDPC Decoders. pages 287{291, 2015. 22nd International Conference on Mixed Design of Integrated Circuits & Systems (MIXDES), Torun, POLAND, JUN 25-27, 2015.	7	0.25	4.642857143
45	Khoa Le, Fakhreddine Ghaffari, Lounis Kessal, David Declercq, Valentin Savin, and Oana Boncalo. Lightweight Hardware Architecture for Probabilistic Gradient Descent Bit Flipping on QC-LDPC Codes. 2018. IEEE International Symposium on Circuits and Systems (ISCAS), Florence, ITALY, MAY 27-30, 2018.	6	0.25	5.416666667
46	Thien Truong Nguyen-Ly, Khoa Le, V. Savin, D. Declercq, F. Ghaffari, and O. Boncalo. Non-Surjective Finite Alphabet Iterative Decoders. 2016. IEEE International Conference on Communications (ICC), Kuala Lumpur, MALAYSIA, MAY 23-27, 2016.	6	0.25	5.416666667

47	Truong Nguyen-Ly, Khoa Le, F. Ghaffari, A. Amaricai, O. Boncalo, V. Savin, and D. Declercq. FPGA Design of High Throughput LDPC Decoder based on Imprecise Offset Min-Sum Decoding. 2015. 13th IEEE International NEW Circuits and Systems Conference, Grenoble, FRANCE, JUN 07-10, 2015.	7	0.25	4.642857143
48	Sergiu Nimara, Alexandru Amaricai, Oana Boncalo, and Mircea Popa. Probabilistic Saboteur-based Simulated Fault Injection Techniques for Low Supply Voltage Interconnects. 2014. 10th Conference on Ph D Research in Microelectronics and Electronics (PRIME), Grenoble, FRANCE, JUN 29-JUL 03, 2014.	4	0.25	8.125
49	Sergiu Nimara, Oana Boncalo, Alexandru Amaricai, and Mircea Popa. FPGA Architecture of Multi-Codeword LDPC Decoder With Efficient BRAM Utilization. pages 52{55, 2016. IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Kosice, SLOVAKIA, APR 20-22, 2016.	4	0.25	8.125
50	Virgil Petcu, Oana Boncalo, Alexandru Amaricai, and Valentin Savin. Variable Throughput LDPC Decoders Using SIMD-based Adaptive Quantization. pages 425{428, 2016. 39th International Conference on Telecommunications and Signal Processing (TSP), Vienna, AUSTRIA, JUN 27-29, 2016	4	0.25	8.125
51	Patricia Carla Petrut, Alexandru Amaricai, and Oana Boncalo. Configurable FPGA Architecture for Hardware-Software Merge Sorting. pages 179{182, 2016. 23rd International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), Lodz, POLAND, JUN 23-25, 2016	3	0.25	10.83333333

	Impact Factor	Punctaj
TOTAL	30.967	610.7144048

Articole ISI în Q1 sau Q2

Nr. crt.	Lucrarea publicată	Q1/Q2	Domain
1	O Boncalo, G Kolumban-Antal, A Amaricai, V Savin, D Declercq "Layered LDPC Decoders With Efficient Memory Access Scheduling and Mapping and Built-In Support for Pipeline Hazards Mitigation" IEEE Transactions on Circuits and Systems I: Regular Papers 66 (4), 2019	Q1	ENGINEERING, ELECTRICAL & ELECTRONIC
2	K Le, D Declercq, F Ghaffari, L Kessal, O Boncalo, V Savin "Variable-node-shift based architecture for probabilistic gradient descent bit flipping on QC-LDPC codes" IEEE Transactions on Circuits and Systems I: Regular Papers 65 (7),2018	Q1	ENGINEERING, ELECTRICAL & ELECTRONIC
3	TT Nguyen-Ly, V Savin, K Le, D Declercq, F Ghaffari, O Boncalo "Analysis and design of cost-effective, high-throughput LDPC decoders" IEEE Transactions on Very Large Scale Integration (VLSI) Systems 26 (3), 2018	Q2	COMPUTER SCIENCE, HARDWARE & ARCHITECTURE
4	D Declercq, V Savin, O Boncalo, F Ghaffari "An imprecise stopping criterion based on in-between layers partial syndromes" IEEE Communications Letters 22 (1), 2018	Q2	TELECOMMUNICATIONS
5	A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	Q2	ENGINEERING, ELECTRICAL & ELECTRONIC

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ȘI A GRADELOR PROFESIONALE DE CERCETARE-DEZVOLTARE

A2 Activitatea de cercetare

A 2.2 Articole în reviste și lucrări în volumele unor manifestări științifice indexate în alte baze de date internaționale recunoscute (BDI)

Candidata: conf. dr. ing. Oana Amaricai-Boncalo

Centralizator Standarde minimale necesare si obligatorii

Nr. crt.	Lucrarea publicată	BDI	Nr. autori	Punctaj
1	Oana Boncalo, Alexandru Amaricai "Two phase reliability analysis of quantum circuits in a block based approach", Elektronika, Vol. 50, No. 2, pp. 90-93, 2010	2	INSPEC	10
2	Alexandru Amaricai, Oana Boncalo "Fault modeling and analysis of short defects in CMOS based reversible circuits" International Journal of Microelectronics and Computer Science, Vol. 1, Issue 2, pp. 175-179, 2010	2	Google Scholar	10
3	Alexandru Amaricai, Oana Boncalo, Ovidiu Sicoe "FPGA Implementations of Low Precision Floating Point Multiply-Accumulate" International Journal of Microelectronics and Computer Science, Vol. 4, Issue 4, pp. 159-164, 2013	3	Google Scholar	6.666666667
4	Oana Boncalo, Mihai Udrescu, Mircea Vladutiu, Lucian Prodan, Alexandru Amaricai "Error-model driven analysis of quantum circuits reliability", Proc. 8th IEEE Conf. on Nanotechnology (NANO), pp. 625-628, 2008	5	IEEE Explore	4
5	Oana Boncalo, Mircea Vladutiu, Alexandru Amaricai "Accuracy analysis of the parallel composition for the block diagram based reliability assessment of quantum circuits" Proc. 2010 Int. Conf. on Computational Cybernetics and Technical Informatics (ICCC-CONTI), pp. 355-359, 2010	3	IEEE Explore	6.666666667
6	Oana Boncalo, Alexandru Amaricai "Logical fault modeling of source drain short defects for CMOS reversible circuits" Proc. 17th Int. Conf. on Mixed Design of Integrated Circuits and Systems (MIXDES), pp. 482-485, 2010	2	IEEE Explore	10
7	Alexandru Amaricai, Alin Dobre, Oana Boncalo, Andrei Tanase, Camelia Valuch "Models and implementations of hardware interface modules in a multi-processor system-on-chip Simulator" Proc. 6th Int. Symposium on Applied Computational Intelligence and Informatics (SACI), pp. 433-437, 2011	5	IEEE Explore	4
8	Oana Boncalo, Alin Dobre, Alexandru Amaricai, Andrei Tanase "A cycle-count-accurate simulation platform with enhanced design exploration capability", Proc. 5th International ICST Conference on Simulation Tools and Techniques (SIMU-TOOLS), pp.113-118,2012	4	ACM	5
9	Alexandru Amaricai, Oana Boncalo "Automatic Generation of FPGA Hardware Accelerators for Graphics Applications" Proc. 2nd International Conference on Pervasive Embedded Computing and Communication Systems, pp. 383-386, 2012	2	DBLP	10
10	Alexandru Amaricai, Constantina Elena Gavriliu, Oana Boncalo "An FPGA sliding window-based architecture harris corner detector" Proc. 24th Int. Conf. on Field Programmable Logic and Applications (FPL), 2014	3	IEEE Explore	6.666666667
11	Oana Boncalo, Alexandru Amaricai, Andrei Hera, Valentin Savin "Cost-efficient FPGA layered LDPC decoder with serial AP-LLR processing" Proc. 24th Int. Conf. on Field Programmable Logic and Applications (FPL), 2014	4	IEEE Explor	5
			TOTAL	78

RAMURA DE ȘTIINȚĂ: CALCULATOARE, TEHNOLOGIA INFORMAȚIEI ȘI INGINERIA SISTEMELOR
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ȘI A GRADELOR PROFESIONALE DE CERCETARE-DEZVOLTARE

A 2.4 Granturi/proiecte de cercetare câștigate prin competiție
A 2.4.1 Director/responsabil partener
A 2.4.1.2 Naționale

Candidata: conf. dr. ing. Oana Amaricai-Boncalo
Centralizator Standarde minimale necesare si obligatorii

Nr. crt.	Grantul/proiectul	Nr. ani	Punctaj
1	Oana Boncalo (director), - "Evaluarea prin simulare a fiabilitatii circuitelor cuantice", TD-25/2007, 2007-2008 - aprox 11000$	2	20
		TOTAL	20

A 2.4.1.2 Internationale

Nr. crt.	Grantul/proiectul	Nr. ani	Punctaj
1	Oana Boncalo (Coordonator Partener Roman), Petru Mihancea, Constantina-Elena Gavriliu, Andrei Hera "DIAMOND - Message Passing Iterative Decoders based on Imprecise Arithmetic for Multi-Objective Power-Area-Delay Optimization" Joint Research Program PNII – IDEI – RO-FR / ANR - Blanc International - Ro: PN-II-ID-JRP-RO-FR-2012-0109 - 148925 Euro	3	60
2	Oana Boncalo, Zsofia Lendek, Proiect cercetare Agentia Spatiala Europeana - Reliable FPGA Datapath Design using Control Techniques -"REDOUBT ESA 4000123993 / 18/NL/CRS" - 48260 Euro (din care UPT-23980 Euro)	1	20
		TOTAL	80

A 2.4.2 Membru în echipă

A 2.4.2.1 Internaționale

Nr. crt.	Grantul/proiectul	Nr. ani	Punctaj
1	Valentin Muresan (Director), Mihai V. Micea (UPT Partner project manager), Alexandru Amaricai-Boncalo, Oana Amaricai-Boncalo, Gheorghe Guran, Andrei Tanase, Valentin Stangaciu, Stangaciu Cristina, Valuch Camelia, Tite Teodor, Ivascu Ancuta-Maria, Velciov Ivan, Vig Adelina, Dura Alexandru, Diaconescu Demis, Cosma Marius, Cretu Vladimir, Vladutiu Mircea, Ciocarlie Horia, Todinca Doru, Prodan Lucian, Mihai Udrescu, "FALX DACIAE: Unelte si Procese de Dezvoltare SW pentru Aplicatii Multimedia Avansate pe Arhitecturi Multi-Core pentru Telefoane Mobile" ("FALX DACIAE: SW Development Tools and Processes for Advanced Multimedia Applications on Mobile Phone Multi-Core Architectures"), POSCCE-A2-O2.1.1 R&D Grant, POSCCE-499-11844/2010 - 2012, EU - Structural Instruments, ANCS - The Romanian National Authority for Scientific Research. Contract 133/04.06.2010. Total value: 2126766 RON (~ 506400 EUR). Value, UPT Partner: 1143416 RON (~ 272300 EUR).	2	8
2	Mircea Popa (UPT Director), Marius Marcu, Sebastian Fuicu, Razvan Bogdan, Oana Boncalo, Marian Salavat, et.al "JCPICS-UDPUT, Joint Cross-Border Internet Communication System of the University of Debrecen and Politehnica University of Timisoara" Hungary-Romania, Hu-Ro	1	4
3	Thomas Fahringer (Coordinator), Marius Marcu (UPT Partner project manager), Sebastian Fuicu, Oana Boncalo, Alexandru Amaricai, Cosmin Cernazanu, Lucian Bara, Madalin Ghenea, et.al "GEMSCLAIM - GreenEr Mobile Systems by Cross LAyer Integrated energy Management", CHIST-ERA, 1/2012	3	12
		TOTAL	24

A 2.4.2.2 Naționale

Nr. crt.	Grantul/proiectul	Nr. ani	Punctaj
1	Mircea Vladutiu (Director), Mihai Udrescu, Lucian Prodan, Oana Boncalo, Alexandru Amaricai "ARHITECTURI BIO-INSPIRATE DE CALCUL PENTRU CIRCUITE LOGICE REVERSIBILE SI CUANTICE", PNII-IDEI-17/2007, 2007-2009	2	4
2	Mihai Udrescu (Director), Mircea Vladutiu, Alexandru Amaricai, Oana Boncalo, Cristian Ruican, Nicola Velciov " PROIECTAREA CIRCUITELOR CUANTICE SI REVERSIBILE TOLERANTE LA DEFECTARE" CNCSIS-380, 207-2008	2	4
		TOTAL	8

RAMURA DE ȘTIINȚĂ: CALCULATOARE, TEHNOLOGIA INFORMAȚIEI ȘI INGINERIA SISTEMELOR
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ȘI A GRADELOR PROFESIONALE DE CERCETARE-DEZVOLTARE

A3 Recunoașterea și impactul activității
A 3.1 Citări în cărți, reviste și volume ale unor manifestări științifice
A 3.1.1 Cărți, ISI

Candidata: conf. dr. ing. Oana Amaricai-Boncalo
Centralizator Standarde minimale necesare si obligatorii

Nr. crt.	Sursa citare	Quarter	Lucarea citată	Nr. autori lucrare citată	Punctaj
1	Dupraz, Elsa; Leduc-Primeau, Francois; Gagnon, Francois "Low-Latency LDPC Decoding Achieved by Code and Architecture Co-Design" 10th IEEE International Symposium on Turbo Codes & Iterative Information Processing (ISTC)		TT Nguyen-Ly, V Savin, K Le, D Declercq, F Ghaffari, O Boncalo "Analysis and design of cost-effective, high-throughput LDPC decoders" IEEE Transactions on Very Large Scale Integration (VLSI) Systems 26 (3), 508-521, 2018	6	1.33333
2	Roberts, Michaelraj Kingston "Simulation and implementation design of multi-mode decoder for WiMAX and WLAN applications " Measurement, 2019	Q2	O Boncalo, A Amaricai, PF Mihancea, V Savin "Memory trade-offs in layered self-corrected min-sum LDPC decoders" Analog Integrated Circuits and Signal Processing 87 (2), 169-180	4	4
3	Liu, Yanhuan; Zhang, Chun; Song, Pengcheng; et al. "A High-Performance FPGA-based LDPC Decoder for Solid-State Drives" Proc. 60th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) , 2018		V Petcu, O Boncalo, A Amaricai, V Savin "Variable throughput LDPC decoders using SIMD-based adaptive quantization" 2016 39th International Conference on Telecommunications and Signal Processing (TSP)	4	2
4	Xie, Tianjiao; Li, Bo; Yang, Mao; et al. "Memory Compact High-Speed QC-LDPC Decoder" IEEE International Conference on Signal Processing, Communications and Computing (ICSPCC), 2017		S Nimara, O Boncalo, A Amaricai, M Popa "FPGA architecture of multi-codeword LDPC decoder with efficient BRAM utilization" 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)	4	2
5	Radhika, V.; Baskaran, K. "FPGA Based DPWM/DPFM Architecture for Digitally Controlled DC-DC Converters" IEEE-Uttar-Pradesh-Section International Conference on Electrical, Computer, and Electronics Engineering (UPCON) . 2016		S Nimara, O Boncalo, A Amaricai, M Popa "FPGA architecture of multi-codeword LDPC decoder with efficient BRAM utilization" 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)	4	2
6	Mahony, Aidan O.; Popovici, Emanuel " Power analysis of sorting algorithms on FPGA using OpenCL " 29th Irish Signals and Systems Conference (ISSC), 2017		PC Petrut, A Amaricai, O Boncalo "Configurable fpga architecture for hardware-software merge sorting" 2016 MIXDES-23rd International Conference Mixed Design of Integrated Circuits and Systems	3	2.66667
7	Sadangi, Sushant; Priyanka, Priti "FPGA Implementation of Parallel Sorting Mechanism for Turbo Decoding in LTE System" International Conference on Inventive Communication and Computational Technologies (ICICCT) , 2019		PC Petrut, A Amaricai, O Boncalo "Configurable fpga architecture for hardware-software merge sorting" 2016 MIXDES-23rd International Conference Mixed Design of Integrated Circuits and Systems	3	2.66667
8	Alimi, Nejmeddine; Machhout, Mohsen; Lahbib, Younes; et al. "An RTOS-based Fault Injection Simulator for Embedded Processors" INTERNATIONAL JOURNAL OF ADVANCED COMPUTER SCIENCE AND APPLICATIONS, 2017		S Nimara, A Amaricai, O Boncalo, M Popa "Multi-Level Simulated Fault Injection for Data Dependent Reliability Analysis of RTL Circuit Descriptions" ADVANCES IN ELECTRICAL AND COMPUTER ENGINEERING 16 (1), 93-98	4	2
9	Dupraz, Elsa; Declercq, David; Vasic, Bane " Asymptotic Error Probability of the Gallager B Decoder Under Timing Errors" IEEE COMMUNICATIONS LETTERS , 2017	Q2	A Amaricai, V Savin, O Boncalo, N Cucu-Laurenciu, J Chen, S Cotofana "Timing error analysis of flooded LDPC decoders" 2015 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS), 2015	6	2.66667
10	Ahmed, Adel A.; Alzahrani, Ahmad A. " A comprehensive survey on handover management for vehicular ad hoc network based on 5G mobile networks technology" TRANSACTIONS ON EMERGING TELECOMMUNICATIONS TECHNOLOGIES, 2019		T Nguyen-Ly, K Le, F Ghaffari, A Amaricai, O Boncalo, V Savin,D. Declercq "FPGA design of high throughput LDPC decoder based on imprecise offset min-sum decoding" 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)	7	1.14286
11	Vural, Hulya; Koyuncu, Murat; Guney, Sinem "A Systematic Literature Review on Microservices" 17th International Conference on Computational Science and its Applications (ICCSA), 2017		T Nguyen-Ly, K Le, F Ghaffari, A Amaricai, O Boncalo, V Savin,D. Declercq "FPGA design of high throughput LDPC decoder based on imprecise offset min-sum decoding" 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)	7	1.14286

12	Soua, Ridha; Kalogeiton, Eirini; Manzo, Gaetano; et al. "SDN Coordination for CCN and FC Content Dissemination in VANETs" 8th EAI International Conference on Ad Hoc Networks (ADHOCNETS), 2016		T Nguyen-Ly, K Le, F Ghaffari, A Amaricai, O Boncalo, V Savin,D. Declercq "FPGA design of high throughput LDPC decoder based on imprecise offset min-sum decoding" 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)	7	1.14286
13	Patel, Dharmesh J.; Engineer, Pinalkumar "Design and Implementation of Quasi Cyclic Low Density Parity Check (QC-LDPC) Code on FPGA" 2nd IEEE International Conference on Wireless Communications, Signal Processing and Networking (WiSPNET), 2017		A Amaricai, O Boncalo, I Mot "Memory efficient fpga implementation for flooded ldpc decoder" 2015 23rd Telecommunications Forum Telfor (TELFOR), 500-503	3	2.66667
14	Yuan, Min; Xing, Qianjian; Ma, Zhenguo; et al. " A Fused Continuous Floating-Point MAC on FPGA" IEICE TRANSACTIONS ON FUNDAMENTALS OF ELECTRONICS COMMUNICATIONS AND COMPUTER SCIENCES, 2018		A Amaricai, O Boncalo, CE Gavriliu "Low-precision DSP-based floating-point multiply-add fused for Field Programmable Gate Arrays" IET Computers & Digital Techniques 8 (4), 187-197	3	2.66667
15	Sarma, Rajkumar; Dhariwal, Sandeep; Jain, Shruti "Design and Analysis of a novel 8X8 bit signed/unsigned synchronous MAC architecture using clock gating scheme for fixed-point arithmetic" 2nd International Conference on Intelligent Circuits and Systems (ICICS)		A Amaricai, O Boncalo, CE Gavriliu "Low-precision DSP-based floating-point multiply-add fused for Field Programmable Gate Arrays" IET Computers & Digital Techniques 8 (4), 187-197	3	2.66667
16	Kuang, S-R.; Wu, K-Y. "Low-Energy Instruction Precision Assignment for Multi-mode Multiplier Under Accuracy and Performance Constraints" ARABIAN JOURNAL FOR SCIENCE AND ENGINEERING		A Amaricai, O Boncalo, CE Gavriliu "Low-precision DSP-based floating-point multiply-add fused for Field Programmable Gate Arrays" IET Computers & Digital Techniques 8 (4), 187-197	3	2.66667
17	Brkic, Srdan; Ivanis, Predrag; Vasic, Bane "Majority Logic Decoding Under Data-Dependent Logic Gate Failures" IEEE TRANSACTIONS ON INFORMATION THEORY , 2017	Q2	A Amaricai, S Nimara, O Boncalo, J Chen, E Popovici "Probabilistic gate level fault modeling for near and sub-threshold CMOS circuits" 2014 17th Euromicro Conference on Digital System Design,	5	3.2
18	Dupraz, Elsa; Declercq, David; Vasic, Bane "Asymptotic Error Probability of the Gallager B Decoder Under Timing Errors" IEEE Communication Letters, 2017	Q2	A Amaricai, S Nimara, O Boncalo, J Chen, E Popovici "Probabilistic gate level fault modeling for near and sub-threshold CMOS circuits" 2014 17th Euromicro Conference on Digital System Design,	5	3.2
19	Brkic, Srdan; Ivanis, Predrag; Vasic, Bane "Reliability of Memories Built From Unreliable Components Under Data-Dependent Gate Failures" IEEE COMMUNICATIONS LETTERS, 2015	Q2	A Amaricai, S Nimara, O Boncalo, J Chen, E Popovici "Probabilistic gate level fault modeling for near and sub-threshold CMOS circuits" 2014 17th Euromicro Conference on Digital System Design,	5	3.2
20	Brkic, Srdan; Al Rasheed, Omran; Ivanis, Predrag; et al. " On Fault Tolerance of the Gallager B Decoder Under Data-Dependent Gate Failures" IEEE COMMUNICATIONS LETTERS, 2015	Q2	A Amaricai, S Nimara, O Boncalo, J Chen, E Popovici "Probabilistic gate level fault modeling for near and sub-threshold CMOS circuits" 2014 17th Euromicro Conference on Digital System Design,	5	3.2
21	Brkic, Srdan; Ivanis, Predrag; Vasic, Bane " Hard-Decision Decoding of LDPC Codes Under Timing Errors: Overview and New Results" 25th Telecommunication Forum (TELFOR) , 2017		A Amaricai, S Nimara, O Boncalo, J Chen, E Popovici "Probabilistic gate level fault modeling for near and sub-threshold CMOS circuits" 2014 17th Euromicro Conference on Digital System Design,	5	1.6
22	Dupraz, Elsa; Vasic, Bane; Declercq, David "Performance of Taylor-Kuznetsov Memories Under Timing Errors" IEEE International Conference on Communications (ICC), 2017		A Amaricai, S Nimara, O Boncalo, J Chen, E Popovici "Probabilistic gate level fault modeling for near and sub-threshold CMOS circuits" 2014 17th Euromicro Conference on Digital System Design,	5	1.6
23	Brkic, Srdan; Ivanis, Predrag; Vasic, Bane " Guaranteed Error Correction of Faulty Bit-Flipping Decoders under Data-Dependent Gate Failures" IEEE International Symposium on Information Theory (ISIT) , 2016		A Amaricai, S Nimara, O Boncalo, J Chen, E Popovici "Probabilistic gate level fault modeling for near and sub-threshold CMOS circuits" 2014 17th Euromicro Conference on Digital System Design,	5	1.6
24	Wilson, David; Shastri, Aniruddha; Stitt, Greg "A High-Level Synthesis Scheduling and Binding Heuristic for FPGA Fault Tolerance" INTERNATIONAL JOURNAL OF RECONFIGURABLE COMPUTING		O Boncalo, A Amaricai, C Spagnol, E Popovici "Cost effective FPGA probabilistic fault emulation" 2014 NORCHIP	4	2
25	Xu, Song; Liu, Qiang; Li, Tao; et al. " IC Security Evaluation against Fault Injection Attack Based on FPGA Emulation" 15th International Conference on Field-Programmable Technology (FPT), 2016		O Boncalo, A Amaricai, C Spagnol, E Popovici "Cost effective FPGA probabilistic fault emulation" 2014 NORCHIP	4	2
26	Quinn, Heather; Wirthlin, Michael "Validation Techniques for Fault Emulation of SRAM-based FPGAs" IEEE TRANSACTIONS ON NUCLEAR SCIENCE , 2015	Q1	O Boncalo, A Amaricai, C Spagnol, E Popovici "Cost effective FPGA probabilistic fault emulation" 2014 NORCHIP	4	4
27	Peng Yuanxi; Chen Jiyang; Lei Yuanwu; et al. "Low-Latency SRT Division and Square Root Based on Remainder and Quotient Prediction" CHINESE JOURNAL OF ELECTRONICS , 2017		A Amaricai, O Boncalo "SRT radix-2 dividers with (5, 4) redundant representation of partial remainder" 2013 NORCHIP,	2	4
28	Geier, Martin; Pitzl, Florian; Chakraborty, Samarjit "GigE Vision Data Acquisition for Visual Servoing using SG/DMA Proxying" 14th ACM/IEEE Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia)		A Amaricai, O Boncalo, M Iordate, B Marinescu "A moving window architecture for a hw/sw codesign based Canny edge detection for FPGA" 2012 28th International Conference on Microelectronics	4	2

29	Bai, Vadithe Madhu; Sailaja, M. "An Efficient Modified Booth Recoder for Different Applications" International Conference on Communication and Electronics Systems (ICCES), 2016		A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	2.66667
30	Singh, Naginder; Sasamal, Trailokya Nath "Design and Synthesis of Goldschmidt Algorithm based Floating Point Divider on FPGA" 2016 INTERNATIONAL CONFERENCE ON COMMUNICATION AND SIGNAL PROCESSING (ICCSP)		A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	2.66667
31	Swamy, K. N. Narendra; Suman, J. Venkata " Design of Optimized Multiply Accumulate Unit Using EMBR Techniques for Low Power Applications" 2nd International Conference on Computational Intelligence in Data Mining (ICCIDM), 2016		A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	2.66667
32	Durgadevi, S.; Seshasayanan, R. "VLSI Implementation of an efficient Fused Add-Multiply Unit using Constant-time addition" 2015 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS)		A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	2.66667
33	Srinitha, S.; Sargunam, B. "Area Effective and Speed Optimized Fused Add-Multiply Unit" 2015 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS)		A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	2.66667
34	Shruthilaya, K.; Vinoth, M. "Power Estimation of Modified Booth Recoder for Efficient Add-Multiply Operator" 2nd International Conference on Computing for Sustainable Global Development (INDIACom) , 2015		A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	2.66667
35	Tsoumanis, Kostas; Xydis, Sotiris; Efstathiou, Constantinos; et al. "An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS, 2014	Q2	A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	5.33333
36	Pham, Tranbichthuan; Wang, Yi; Li, Renfa "A variable-latency Floating-point Division in Association with Predicted Quotient and Fixed Remainder" IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), 2013		A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	2.66667
37	Velasco, Alejandro David; Montrucchio, Bartolomeo; Rebaudengo, Maurizio "KITO tool: A fault injection environment in Linux kernel data structures", Microelectronics Reliability, 2016		O Boncalo, A Amăricăi, M Udrescu, M Vlăduţiu "Quantum circuit's reliability assessment with VHDL-based simulated fault injection" Microelectronics Reliability 50 (2)	4	2
38	Frechtling, Michael; Leong, Philip H. W. "MCALIB: Measuring Sensitivity to Rounding Error with Monte Carlo Programming" ACM TRANSACTIONS ON PROGRAMMING LANGUAGES AND SYSTEMS		A Amaricai, M Vladutiu, O Boncalo "Design of floating point units for interval arithmetic" 2009 Ph. D. Research in Microelectronics and Electronics	3	2.66667
39	Arun, Konduri; Srivatsan, K. "A Binary High Speed Floating Point Multiplier" 2017 INTERNATIONAL CONFERENCE ON NEXTGEN ELECTRONIC TECHNOLOGIES: SILICON TO SOFTWARE (ICNETS2), 2017		A Amaricai, M Vladutiu, M Udrescu, L Prodan, O Boncalo "Floating point multiplication rounding schemes for interval arithmetic" 2008 International Conference on Application-Specific Systems, Architectures and Processors	5	1.6
40	Bruguera, Javier D. "Optimizing the representation of intervals" SCIENCE OF COMPUTER PROGRAMMING, 2014		A Amaricai, M Vladutiu, M Udrescu, L Prodan, O Boncalo "Floating point multiplication rounding schemes for interval arithmetic" 2008 International Conference on Application-Specific Systems, Architectures and Processors	5	1.6
41	Garcia, Hector J.; Markov, Igor L. "Simulation of Quantum Circuits via Stabilizer Frames" IEEE TRANSACTIONS ON COMPUTERS , 2015	Q1	O Boncalo, M Udrescu, L Prodan, M Vladutiu, A Amaricai "Using simulated fault injection for fault tolerance assessment of quantum circuits" 40th Annual Simulation Symposium (ANSS'07), 213-220	5	3.2
42	Garcia, Hector J.; Markov, Igor L. " Quipu: High-performance Simulation of Quantum Circuits using Stabilizer Frames" 2013 IEEE 31ST INTERNATIONAL CONFERENCE ON COMPUTER DESIGN (ICCD)		O Boncalo, M Udrescu, L Prodan, M Vladutiu, A Amaricai "Using simulated fault injection for fault tolerance assessment of quantum circuits" 40th Annual Simulation Symposium (ANSS'07), 213-220	5	1.6
43	Akkas, Ahmet "Dual-mode floating-point adder architectures" JOURNAL OF SYSTEMS ARCHITECTURE, 2008		A Amaricai, M Vladutiu, L Prodan, M Udrescu, O Boncalo "Design of addition and multiplication units for high performance interval arithmetic processor" 2007 IEEE Design and Diagnostics of Electronic Circuits and Systems	5	1.6
44	Hamid, Lamiaa S. A.; Shehata, Khaled A.; El-Ghitani, Hassan; et al. "Design of Generic Floating Point Multiplier and Adder/Subtractor Units" 2010 12TH INTERNATIONAL CONFERENCE ON COMPUTER MODELLING AND SIMULATION (UKSIM)		A Amaricai, M Vladutiu, L Prodan, M Udrescu, O Boncalo "Design of addition and multiplication units for high performance interval arithmetic processor" 2007 IEEE Design and Diagnostics of Electronic Circuits and Systems	5	1.6
				TOTAL	106.895

RAMURA DE ȘTIINȚĂ: CALCULATOARE, TEHNOLOGIA INFORMAȚIEI ȘI INGINERIA SISTEMELOR
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ȘI A GRADELOR PROFESIONALE DE CERCETARE-DEZVOLTARE

A3 Recunoașterea și impactul activității
A 3.1 Citări în cărți, reviste și volume ale unor manifestări științifice
A 3.1.2 BDI

Candidata: conf. dr. ing. Oana Amaricai-Boncalo
Centralizator Standarde minimale necesare si obligatorii

Nr. crt.	Sursa citare	BDI	Lucarea citată	Nr. autori lucrare citată	Punctaj
1	Wang, B., Mu, J., Jiao, X., Wang, Z. - "Method for early termination of ADMM penalized decoding for LDPC codes " Journal of Xidian University, 2019	Scopus	D Declercq, V Savin, O Boncalo, F Ghaffari "An imprecise stopping criterion based on in-between layers partial syndromes" IEEE Communications Letters 22 (1), 2018	4	1
2	Suud, J., Zen, H., Hj Othman, A.-K.B., Hamid, K.A. "Decoding of decode and forward (DF) relay protocol using min-sum based low density parity check (LDPC) system" International Journal of Communication Networks and Information Security, 2018	Scopus	TT Nguyen-Ly, V Savin, K Le, D Declercq, F Ghaffari, O Boncalo "Analysis and design of cost-effective, high-throughput LDPC decoders" IEEE Transactions on Very Large Scale Integration (VLSI) Systems 26 (3), 508-521, 2018	6	0.666667
3	Vasic, B., Xiao, X., Lin, S. - "Learning to decode LDPC codes with finite-alphabet message passing"2018 Information Theory and Applications Workshop, ITA 2018	Scopus	TT Nguyen-Ly, V Savin, K Le, D Declercq, F Ghaffari, O Boncalo "Analysis and design of cost-effective, high-throughput LDPC decoders" IEEE Transactions on Very Large Scale Integration (VLSI) Systems 26 (3), 508-521, 2018	6	0.666667
4	Liu, J.-C., Wang, H.-C., Shen, C.-A., Lee, J.-W. "Low-Complexity LDPC Decoder for 5G URLLC" Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics, 2018	Scopus	A Amaricai, O Boncalo "Cost effective FPGA implementation for hard decision LDPC decoders" 2016 24th Telecommunications Forum (TELFOR)	2	2
5	Liu, J.-C., Wang, H.-C., Shen, C.-A., Lee, J.-W. "Low-Complexity LDPC Decoder for 5G URLLC" Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics, 2018	Scopus	O Boncalo "QC-LDPC Gear-Like Decoder Architecture with Multi-domain Quantization" 2016 Euromicro Conference on Digital System Design (DSD),	1	4
6	Lewandowsky, J., Bauch, G. "Information-Optimum LDPC Decoders Based on the Information Bottleneck Method" IEEE Access, 2018	Scopus	TT Nguyen-Ly, K Le, V Savin, D Declercq, F Ghaffari, O Boncalo "Non-surjective finite alphabet iterative decoders" 2016 IEEE International Conference on Communications (ICC), 2016	6	0.666667
7	Radhika, V., Baskaran, K. "Block-random access memory-based digital pulse modulator architecture for DC–DC converters" 2nd International Conference on Intelligent and Efficient Electrical Systems, ICIEES 2017	Scopus	S Nimara, O Boncalo, A Amaricai, M Popa "FPGA architecture of multi-codeword LDPC decoder with efficient BRAM utilization" 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)	4	1
8	Suud, J., Zen, H., Hj Othman, A.-K.B., Hamid, K.A. "Decoding of decode and forward (DF) relay protocol using min-sum based low density parity check (LDPC) system" International Journal of Communication Networks and Information Security, 2018	Scopus	S Nimara, O Boncalo, A Amaricai, M Popa "FPGA architecture of multi-codeword LDPC decoder with efficient BRAM utilization" 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)	4	1
9	Ren, J., Che, S., Zheng, Z. "Decoding of regular LDPC codes accelerated by the GPU" Journal of Xidian University, 2018	Scopus	O Boncalo, A Amaricai, PF Mihancea, V Savin "Memory trade-offs in layered self-corrected min-sum LDPC decoders" Analog Integrated Circuits and Signal Processing 87 (2), 169-180	4	1
10	Lefter, M., Voicu, G., Marconi, T., Savin, V., Cotofana, S.D. "LDPC-based adaptive multi-error correction for 3D memories" Proceedings - 35th IEEE International Conference on Computer Design, ICCD 2017	Scopus	O Boncalo, PF Mihancea, A Amaricai "Template-based QC-LDPC decoder architecture generation"2015 10th International Conference on Information, Communications and Signal Processing (ICICS)	3	1.333333

11	Dupraz, E., Vasic, B., Declercq, D. "Performance of taylor-kuznetsov memories under timing errors" IEEE International Conference on Communications, 2017	Scopus	A Amaricai, V Savin, O Boncalo, N Cucu-Laurenciu, J Chen, S Cotofana "Timing error analysis of flooded LDPC decoders" 2015 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS), 2015	6	0.666667
12	Wang, B., Mu, J., Jiao, X., Wang, Z. - "Method for early termination of ADMM penalized decoding for LDPC codes " Journal of Xidian University, 2019	Scopus	A Hera, O Boncalo, C-E. Gavriliu, A. Amaricai, V. Savin, D. Declercq, F. Ghaffari "Analysis and implementation of on-the-fly stopping criteria for layered QC LDPC decoders" Proc 2015 22nd International Conference Mixed Design of Integrated Circuits & Systems (MIXDES)	7	0.571429
13	Liu, J.-C., Wang, H.-C., Shen, C.-A., Lee, J.-W. "Low-Complexity LDPC Decoder for 5G URLLC" Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics, 2018	Scopus	T Nguyen-Ly, K Le, F Ghaffari, A Amaricai, O Boncalo, V Savin,D. Declercq "FPGA design of high throughput LDPC decoder based on imprecise offset min-sum decoding" 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)	7	0.571429
14	Petrousov, I., Dasygenis, M. "Automating the generation of hardware accelerators from custom arithmetic functions" ACM International Conference Proceeding Series, 2017	Scopus	T Nguyen-Ly, K Le, F Ghaffari, A Amaricai, O Boncalo, V Savin,D. Declercq "FPGA design of high throughput LDPC decoder based on imprecise offset min-sum decoding" 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)	7	0.571429
15	Sadek, A.M., Hussein, A.I. "Flexible FPGA implementation of Min-Sum decoding algorithm for regular LDPC codes" Proceedings of 2016 11th International Conference on Computer Engineering and Systems, ICCES 2016	Scopus	T Nguyen-Ly, K Le, F Ghaffari, A Amaricai, O Boncalo, V Savin,D. Declercq "FPGA design of high throughput LDPC decoder based on imprecise offset min-sum decoding" 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)	7	0.571429
16	Du, J., Yuan, J., Zhou, L., He, X. "A progressive edge growth algorithm for bit mapping design of LDPC coded BICM schemes" IEEE International Symposium on Information Theory - Proceedings, 2016	Scopus	T Nguyen-Ly, K Le, F Ghaffari, A Amaricai, O Boncalo, V Savin,D. Declercq "FPGA design of high throughput LDPC decoder based on imprecise offset min-sum decoding" 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)	7	0.571429
17	Sarma, R., Dhariwal, S., Jain, S. "Design and analysis of a novel 8X8 bit signed/unsigned synchronous MAC architecture using clock gating scheme for fixed-point arithmetic" Proceedings - 2nd International Conference on Intelligent Circuits and Systems, ICICS 2018	Scopus	A Amaricai, O Boncalo, CE Gavriliu "Low-precision DSP-based floating-point multiply-add fused for Field Programmable Gate Arrays" IET Computers & Digital Techniques 8 (4), 187-197	3	1.333333
18	Hemanandh, S., Subramanian, S. "IEEE 754 compliant floating point fused add sub unit" ARPN Journal of Engineering and Applied Sciences, 2015	Scopus	A Amaricai, O Boncalo, CE Gavriliu "Low-precision DSP-based floating-point multiply-add fused for Field Programmable Gate Arrays" IET Computers & Digital Techniques 8 (4), 187-197	3	1.333333
19	Kim, T., Baik, J., Lee, M., Heo, J. "Adaptive deactivation and zero-forcing scheme for low-complexity LDPC decoders" Eurasip Journal on Wireless Communications and Networking 2017(1),153	Scopus	O Boncalo, A Amaricai, V Savin "Memory efficient implementation of self-corrected min-sum LDPC decoder" Proc. 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2014	3	1.333333
20	Hu, J.-H., Li, X.-Q., Li, Y. "Supply voltage analysis of asymmetry-based MRF circuits via information theory" Journal of the University of Electronic Science and Technology of China, 2016	Scopus	A Amaricai, S Nimara, O Boncalo, J Chen, E Popovici "Probabilistic gate level fault modeling for near and sub-threshold CMOS circuits" 2014 17th Euromicro Conference on Digital System Design,	5	0.8
21	Vasić, B., Ivaniš, P., Brkic, S. "Low complexity memory architectures based on LDPC codes: Benefits and disadvantages" 2015 12th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services, TELSIKS 2015	Scopus	A Amaricai, S Nimara, O Boncalo, J Chen, E Popovici "Probabilistic gate level fault modeling for near and sub-threshold CMOS circuits" 2014 17th Euromicro Conference on Digital System Design,	5	0.8
22	Pham, T.H., Tran, P., Lam, S.-K. "High-Throughput and Area-Optimized Architecture for rBRIEF Feature Extraction" IEEE Transactions on Very Large Scale Integration (VLSI) Systems 27(4), 2019	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333

23	Ben Amara, A., Pissaloux, E., Grisel, R., Atri, M. "Zynq FPGA based memory efficient and real-time harris corner detection algorithm implementation" 2018 15th International Multi-Conference on Systems, Signals and Devices, SSD 2018	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
24	Jasani, B.A., Lam, S.-K., Meher, P.K., Wu, M. "Threshold-Guided Design and Optimization for Harris Corner Detector Architecture" IEEE Transactions on Circuits and Systems for Video Technology 28(12), 2018	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
25	Chahuara, H., Rodriguez, P. "Real-Time Corner Detection on Mobile Platforms Using Cuda" Proceedings of the 2018 IEEE 25th International Conference on Electronics, Electrical Engineering and Computing, INTERCON 2018	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
26	Liu, S., Lyu, C., Liu, Y., Chen, H., Li, Y. "Real-time implementation of harris corner detection system based on FPGA" 2017 IEEE International Conference on Real-Time Computing and Robotics, RCAR 2017	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
27	Aguilar-González, A., Arias-Estrada, M., Berry, F. " Robust feature extraction algorithm suitable for real-time embedded applications" Journal of Real-Time Image Processing 14(3), pp. 647-665, 2018	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
28	Lam, S.-K., Bijarniya, R.K., Wu, M. "Lowering dynamic power in stream-based harris corner detection architecture" 2017 International Conference on Field-Programmable Technology, ICFPT 2017	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
29	Zhang, S., Wang, Y. "Design for an accelerated harris feature point extraction system base on all programmable system on chip" 2017 4th International Conference on Systems and Informatics, ICSAI 2017	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
30	Qasaimeh, M., Zambreno, J., Jones, P.H. "A modified sliding window architecture for efficient BRAM resource utilization" 2017 IEEE 31st International Parallel and Distributed Processing Symposium Workshops, IPDPSW 2017	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
31	Changan, K.S., Chilveri, P.G. "Stereo image feature matching using Harris corner detection algorithm" International Conference on Automatic Control and Dynamic Optimization Techniques, ICACDOT 2016	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
32	Ahmed, H., Sidek, O. "An energy-aware self-adaptive System-on-Chip architecture for real-time Harris corner detection with multi-resolution support" Microprocessors and Microsystems, 2017	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
33	Schulz, V.H., Bombardelli, F.G., Todt, E. "A SoC with FPGA Landmark Acquisition System for Binocular Visual SLAM" Proceedings - 12th LARS Latin American Robotics Symposium and 3rd SBR Brazilian Robotics Symposium, LARS-SBR 2015 - Part of the Robotics Conferences 2015	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
34	Orabi, H., Shaikh-Husin, N., Sheikh, U.U. "Low cost pipelined FPGA architecture of Harris Corner Detector for real-time applications" The 10th International Conference on Digital Information Management, ICDIM 2015	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
35	Schulz, V.H., Bombardelli, F.G., Todt, E. "A harris corner detector implementation in SoC-FPGA for visual SLAM" Communications in Computer and Information Science 619, pp. 57-71, 2016	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333

36	Chen, L., Han, J., Zhang, Y., Bai, L.-F. "Real-time panoramic image mosaic via harris corner detection on FPGA" Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 2015	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
37	Chao, T.L., Wong, K.H. "An efficient FPGA implementation of the Harris corner feature detector" Proceedings of the 14th IAPR International Conference on Machine Vision Applications, MVA 2015 7153140, pp. 89-93	Scopus	A Amaricai, CE Gavriliu, O Boncalo "An FPGA sliding window-based architecture harris corner detector" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	3	1.333333
38	Andrade, J., George, N., Karras, K., et.al "Design Space Exploration of LDPC Decoders Using High-Level Synthesis" IEEE Access, 2017	Scopus	O Boncalo, A Amaricai, A Hera, V Savin "Cost-efficient FPGA layered LDPC decoder with serial AP-LLR processing" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	4	1
39	Wu, Z., Su, K. "Updating conflict solution for pipelined layered LDPC decoder" 2015 IEEE International Conference on Signal Processing, Communications and Computing, ICSPCC 2015	Scopus	O Boncalo, A Amaricai, A Hera, V Savin "Cost-efficient FPGA layered LDPC decoder with serial AP-LLR processing" 2014 24th International Conference on Field Programmable Logic and Applications (FPL)	4	1
40	Beasley, A.E., Watson, R.J., Clarke, C.T. "Efficient digital implementation of a multi-precision square-root algorithm" IET Computers and Digital Techniques, 2019	Scopus	A Amaricai, O Boncalo "FPGA implementation of very high radix square root with prescaling" Proc. 2012 19st IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2012	2	2
41	Aruna Manjusha, K., Naresh, B., Arulanath, T.S. "A new architecture of modified booth recorder for add multiply operator using carry save adder" ARPN Journal of Engineering and Applied Sciences 13(6), pp. 2153-2156, 2018	Scopus	A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	1.333333
42	Kamble, L., Palsodkar, P., Palsodkar, P. "Research trends in development of floating point computer arithmetic" Proceedings of the 2017 IEEE International Conference on Communication and Signal Processing, ICCSP 2017	Scopus	A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	1.333333
43	Krishnamoorthy, R., Sujetha, B., Saravanan, S., Haridevi, P. "A low power recoding methodology for the design of a MAC unit using fused architecture" Pakistan Journal of Biotechnology 13, pp. 212-214, 2016	Scopus	A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	1.333333
44	Lokeshwari, V., Vardhan, V. "Modified booth recoding for complex arithmetic operation in DSP application" International Journal of Applied Engineering Research 10(9), pp. 22385-22392, 2015	Scopus	A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	1.333333
45	Sanju, I.M.S. "Design and implementation of efficient modified booth recoder and wallace tree for the FAM operator" International Journal of Applied Engineering Research, 2015	Scopus	A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	1.333333
46	Senthurpandiyan, K., Mahendren, G. "An optimized booth recoder for efficient design of the add-multiply operator" International Journal of Applied Engineering Research 10(55), pp. 953-956, 2015	Scopus	A Amaricai, M Vladutiu, O Boncalo "Design issues and implementations for floating-point divide–add fused" IEEE Transactions on Circuits and Systems II: Express Briefs 57 (4)	3	1.333333
47	Daoud, L., Zydek, D., Selvaraj, H. "A Survey on Design and Implementation of Floating Point Adder in FPGA" Advances in Intelligent Systems and Computing 1089, pp. 885-892, 2015	Scopus	A Amaricai, M Vladupiu, L Prodan, M Udrescu, O Boncalo "Exploiting parallelism in double path adders' structure for increased throughput of floating point addition"	5	0.8
48	Zheng, Q., Li, Z., Ye, J., Wei, C., Chen, J. "Implementation of an instruction dispatch unit applied to digital signal processors with VLIW architecture" 2010 2nd Pacific-Asia Conference on Circuits, Communications and System, PACCS 2010	Scopus	A Amaricai, M Vladupiu, L Prodan, M Udrescu, O Boncalo "Exploiting parallelism in double path adders' structure for increased throughput of floating point addition"	5	0.8
				TOTAL	57.39048

RAMURA DE ȘTIINȚĂ: CALCULATOARE, TEHNOLOGIA INFORMAȚIEI ȘI INGINERIA SISTEMELOR
STANDARDE MINIMALE ȘI OBLIGATORII PENTRU CONFERIREA TITLURILOR DIDACTICE DIN ÎNVĂȚĂMÂNTUL SUPERIOR ȘI A GRADELOR PROFESIONALE DE CERCETARE-DEZVOLTARE

A 3.2 Membru în comitetele de redacție sau comitelele științifice ale revistelor indexate ISI, chair, co-chair sau membru în comitetele de organizare ale manifestărilor științifice internaționale indexate ISI

Candidata: conf. dr. ing. Oana Amaricai-Boncalo

Centralizator Standarde minimale necesare si obligatorii

Nr. crt.	Activitatea	Punctaj
1	Handling Editor, Microprocessors and Microsystem (Jurnal ISI IF 1.039), 2017-2019	10
	TOTAL	10

A 3.2 Membru în comitetele de redacție sau comitelele științifice ale revistelor indexate ISI, chair, co-chair sau membru în comitetele de organizare ale manifestărilor științifice internaționale indexate BDI

Nr. crt.	Activitatea	Punctaj
1	Membru comitet tehnic de program, IEEE International Conference on Computer and Information Technology, 2008.	6
2	Membru comitet tehnic de program, IEEE International Conference on Computer and Information Technology, 2009.	6
3	Membru comitet tehnic de program, IEEE International Conference on Computer and Information Technology, 2010.	6
4	Membru comitet tehnic de program, IEEE International Conference on Computer and Information Technology, 2011.	6
5	Membru comitet tehnic de program, Euromicro DSD, 2018.	6
	TOTAL	30

RAMURA DE ȘTIINȚĂ: CALCULATOARE, TEHNOLOGIA INFORMAȚIEI ȘI INGINERIA SISTEMELOR
STANDARDE MINIMALE ȘI OBLIGATORII PENTRU CONFERIREA TITLURILOR DIDACTICE DIN ÎNVĂȚĂMÂNTUL SUPERIOR
ȘI A GRADELOR PROFESIONALE DE CERCETARE-DEZVOLTARE

A 3.4 Premii în domeniu conferite de Academia Română, ASTR, AOSR, sau premii internaționale de prestigiu

Candidata: conf. dr. ing. Oana Amaricai-Boncalo

Centralizator Standarde minimale necesare si obligatorii

Nr. crt.	Premiul decernat	Punctaj
1	Poland Section IEEE ED Chapter Young Scientist Award, MIXDES Conference 2016	15
	TOTAL	15