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RESEARCH ON SOLDER JOINT LIFETIME OF SURFACE-MOUNTED DEVICES

Teză de doctorat – Rezumat

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1 Introduction

During their lifetime, the electronic devices undergo slow-changing temperature variations – thermal cycling in Figure 1 (b), rapidly changing temperature variations – thermal shock cycles, and vibration cycles. Thermal cycling-induced failures, such as cracks in solder balls, shown in Figure 1 (a, c), are a prevalent reliability concern [1]. Thermal expansion mismatch between the electronic components and PCBs leads to stress and strain in solder joints. As a result, the solder joints respond through time-dependent plastic deformation, accumulating over time, eventually leading to the apparition of cracks, as in Figure 1 (c), and product malfunction. Across the electronics industry, solder joint-related issues cause 13% of failures [2], and high-temperature conditions and temperature cycling is the main reason [1]. In the past twenty years, with the increasing complexity of vehicles, the number of auto recalls doubled, and in 2015, electronics covered 6% of vehicle recalls. Furthermore, autonomous driving imposes a zero-defect mindset, which underlines the need for quality strategy improvement, focused on prevention and defect elimination [3].

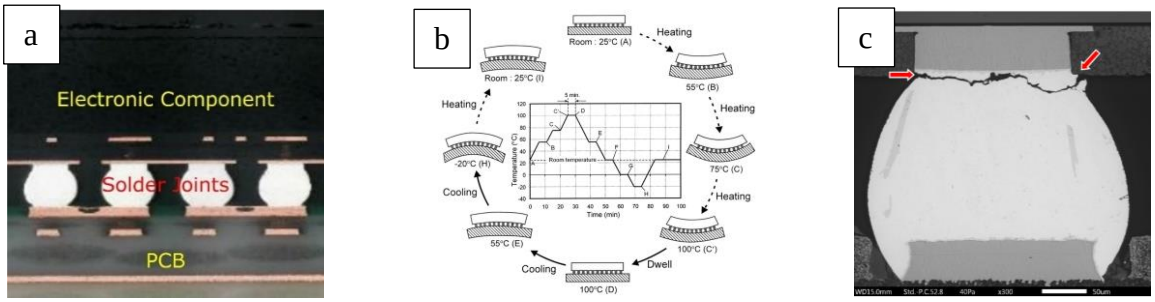

Figure 1 Cross-section of an electronic part mounted on a PCB (a). Illustration of the deformation of an IC – PCB assembly during thermal cycling. Reproduced with permission from S. Cho, ASME Journal of Electronic Packaging, 2004, vol. 126(1): 41-47 [4] (b). Solder joint fatigue crack. Image used courtesy of Continental AG (c).

The motivation for this work comes from the need for a continuous quality improvement strategy in developing electronics for autonomous driving. Electronic part manufacturers test their products based on current standards [5] and for their intended use through board-level reliability (BLR) testing. However, in a PCB that is part of a product (or system), the stress state in the solder joints changes due to added loads such as fixations [6] [7]. The increased mechanical stress can accelerate the solder joint failure. The proposed methodology involves board-level experimental, analytical, and numerical calibration. The goal is to develop a standardized simulation workflow for predictive system-level reliability (SLR) assessment.

2 Literature Review

Dudek [8] defines two fundamental approaches in solder joint reliability assessment: theoretical and experimental approaches. The scope of the reliability test is to obtain failures on a statistically significant number of samples and determine the life distribution. The statistical distribution of solder joint failures follows a two-parameter Weibull distribution defined by the scale parameter, θ, and the slope or shape parameter, β. Qualification tests evaluate if a product passes or not a specific test threshold. They have a predefined duration and aim to qualify a particular design. Qualification tests include a smaller sample size than reliability tests and render fewer failures [9]. Typically, solder reliability testing considers different accelerated temperature profiles in an Accelerated Thermal Cycling (ATC) test.

The theoretical board-level reliability assessment approach uses a fatigue model to predict the failure of solder joints. *The Engelmaier – Wild* [10] model in (1) estimates the leadless components' mean fatigue life by considering the solder's cyclic total plastic shear strain range after complete relaxation.

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma}{2\varepsilon_f'}\right]^{\frac{1}{c}} \tag{1}$$

$$\Delta\gamma = C\frac{L_D}{h}\Delta(\alpha\Delta T) \tag{2}$$

$$c = c_0 + c_1 * \overline{T_{SJ}} + c_2 * 10^{-2}\ln\left(1 + \frac{t_0}{t_D}\right) \tag{3}$$

$$L_D = \frac{1}{2}\sqrt{L^2 + W^2} \tag{4}$$

where ε_f' is the fatigue ductility coefficient, c is the fatigue ductility exponent determined with (3), T_{SJ} is the mean cyclic solder joint temperature, $T_{SJ} = 1/4(T_c + T_s + 2T_0)$, T_c, T_s are the steady-state temperatures for component (c) and substrate (s), T_0 is the temperature during off half-cycle, t_D is the half-cycle dwell time, C is an empirical "nonideal" factor, L_D is the distance from the neutral axis of the assembly to the outermost solder joint as in (4), h is the solder joint height, α is the coefficient of thermal expansion and ΔT is the temperature range.

The Ansys® Sherlock software calculates the shear strain range according to (2) and then calculates the shear force on the solder joint using equation (5) [11]. Lastly, the application uses the prediction model in (6) to determine the cycles to failure, where W' and m'' take the default values fitted by Syed in [12].

$$(\alpha_2 - \alpha_1)\Delta T L_D = F\left(\frac{L_D}{E_1A_1} + \frac{L_D}{E_2A_2} + \frac{h_s}{A_sG_s} + \frac{h_c}{A_cG_c} + \left(\frac{2-\nu}{9G_ba}\right)\right) \tag{5}$$

$$N_f = (W' w_{cr}^{acc})^{-m''} \tag{6}$$

where α, ΔT and L_D are the same parameters as in (2), E is the elastic modulus, G is the shear modulus, A is the area, h is the height, and a is the edge length of the bond pad. Subscripts 1 stands for component, 2 and b for the PCB, s for solder joint, and c for bond pad [13].

The *numerical approach* involves a nonlinear transient thermomechanical finite element analysis (FEA). Different creep laws describe the behavior of the solder alloy. In post-processing, the engineer introduces the calculated solder joint response in a life prediction equation to determine the cycles to failure. The Hyperbolic sine creep model in (7) and its form as the Garofalo model ready to implement in Ansys Mechanical in (8) is a widely adopted model for SAC alloys as fitted by Schubert et al. [14]. Table 1 shows the model parameters and four life prediction equations for creep strain and energy criteria. We use the energy-based models referred to as the Schubert model [14] and the Syed model [12].

$$\frac{d\varepsilon_{cr}}{dt} = A_1[sinh(\alpha\sigma)]^n exp\left(\frac{-Q_1}{RT}\right) \tag{7}$$

$$\frac{d\varepsilon_{cr}}{dt} = C_1[sinh(C_2\sigma)]^{C_3} exp\left(\frac{-C_4}{T}\right) \tag{8}$$

Parameter	**A1 (s^{-1})**	**α (MPa^{-1})**	**n**	**Q1/R**	**E (MPa)**
	C1	**C2**	**C3**	**C4**	**ν; α (ppm/K)**
Sn3.8Ag0.7Cu Sn3.5Ag0.75Cu Sn3.5Ag0.5Cu Castin™ [14]	277984	0.02447	6.41	6500	E=61251–58.5T ν=0.36; α=20
$N_f = 345(w_{cr}^{acc})^{(-1.02)}$ [14] $N_f = 4.5(\varepsilon_{cr}^{acc})^{(-1.295)}$ [14] $N_f = (0.0019w_{cr}^{acc})^{-1}$ [12] $N_f = (0.0069w_{cr}^{acc})^{-1}$ [15]					

Table 1 The Hyperbolic sine (Garofalo) constitutive equation (7) (8) and parameter values, and related life prediction models.

In the strain energy density ratio (SEDR) approach, the failure of a solder joint occurs when the accumulated strain energy density ratio exceeds a specific critical value. The SEDR approach considers the strain energy density accumulated in the solder joint due to various loading conditions. Based on the Coffin-Manson lifetime model in (9), SEDR takes the form in (10), where the subscript FailBaseCycle denotes the critical failure cycle and corresponding dissipated energy density [11]. SEDR is suitable for SLR, as it allows some modeling freedom compared to empirical prediction models, which require strict modeling rules [16].

$$N_f = \Theta_2(W_{cr}^{acc})^{-c2} \tag{9}$$

$$N_f = N_{FailBaseCycle}\left(\frac{W_{cr}^{acc}}{W_{cr,FailBaseCycle}^{acc}}\right)^{-c2} \tag{10}$$

3 Methodology and Results

In order to develop a solution for the identified problem, the research methodology aims to answer the following research questions:

- How can virtual prototyping be used to improve the reliability of electronics?
- How can the stress state in solder joints be evaluated in the context of the system they are part of, moving from board-level to system-level reliability assessment?
- Can a simulation workflow be developed for system-level reliability assessment?

The research hypothesis is that one can create a simulation workflow for system-level reliability assessment by calibrating the simulation models at the board level. Following the developed workflow, the system-level analysis can identify the solder connections at risk of failure and suggest improvements.

In addition, to develop the workflow, the research collects qualitative data and combines quantitative and qualitative research methods. The qualitative research methods used in this study include interviews and discussions with experts within the Continental organization (Romania, Germany, USA, Singapore, and India) and industry (NXP, Infineon, Xilinx, Micron, Renesas, AT&S), and academic and research members (Fraunhofer Institute, PCCL, Politehnica University from Bucharest, Politehnica University from Timisoara), focus group discussion within Continental, and a document analysis of relevant literature. The focus group discusses the challenges and approaches in solder joint reliability assessment. The document analysis involved reviewing relevant literature on the reliability assessment of electronics. The network within the company involves experts in various disciplines, such as FEA, simulation and validation, thermal analysis, complex packaging, soldering and new product launch. The focus groups include FEA specialists and experts. Within the research activities, a communication channel opened with part suppliers, packaging experts and experienced simulation engineers on the suppliers' side.

A potential research limitation includes the need for previous experience in the field, potentially leading to overlooking specific factors that more experienced researchers might have considered and formulating inaccurate assumptions due to lack of experience. Most data collection and analysis is cost-effective as independent research without specific funding or research project.

The mitigation of this potential bias included consulting with experts in the field and attending conferences and courses to broaden the understanding of the research area. However, another potential bias in this study is the selection bias in the qualitative research methods. For example, the experts and the focus group were chosen based on their availability and willingness to participate, which may have resulted in a sample not representative of the entire population of experts in the field. Another potential bias is the confirmation bias in the quantitative research methods, where preconceived ideas about the performance of the packages may have influenced the analysis. To mitigate these biases, we tried to ensure that the research methods were rigorous and objective and that the data was analyzed and interpreted carefully.

The methodology involves experimental and theoretical board-level reliability assessment and calibration, system-level simulation, and the standardization and implementation of the proposed simulation workflow.

In the experimental approach, the test included 16 PCBs with two of each selected component described in Table 2, mounted with SAC305 solder alloy, as in Figure 2. The components come with a daisy chain net topology for testing purposes. The setup takes readings of the electrical resistance of the test point every 10 seconds. The event threshold is 300 Ohms, which means that if the electrical resistance of the test point rises above this level, it will be considered a failure. The temperature cycles from -40°C to +125°C, with a ramp rate of 5°C/min. The minimum and maximum dwell times are 15 min, resulting in a 96-minute cycle, as shown in Figure 3 (left). The experimental BLR test results' data analysis indicates a characteristic life of 162 cycles for the WLP144, 512 cycles for the CVBGA432, respectively of 786 for the CTBGA208, as in Figure 3 (right). The author did not perform the experiments in the thesis but worked for three weeks in the quality assurance laboratory at Continental Temic, Ingolstadt, Germany, to learn the test and cross-section analysis procedures.

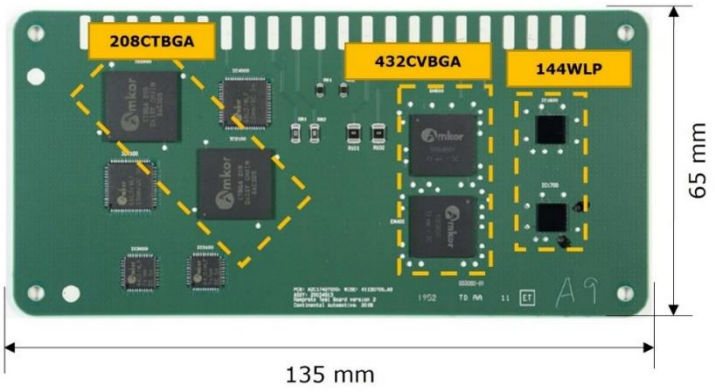

Figure 2 The test board with marked components included in this study. Image used courtesy of Continental AG.

Package	Substrate	Die	Mold	Solder Ball	Pads		Pitch
	LxWxt	LxWxt	t	Dxh	D_{pkg}	D_{PCB}	
WLP144	n/a	5.96x5.96x0.400	n/a	0.256x0.192	0.199	0.247	0.40
CVBGA432	13x13x0.198	9.92x9.92x0.175	0.452	0.254x0.180	0.225	0.200	0.40
CTBGA208	15x15x0.160	12.84x12.84x0.22	0.580	0.419x0.277	0.385	0.331	0.80

Table 2 Package Attributes. All dimensions are in millimeters, mm. L = length, W = width, t = thickness, h = height, D = diameter.

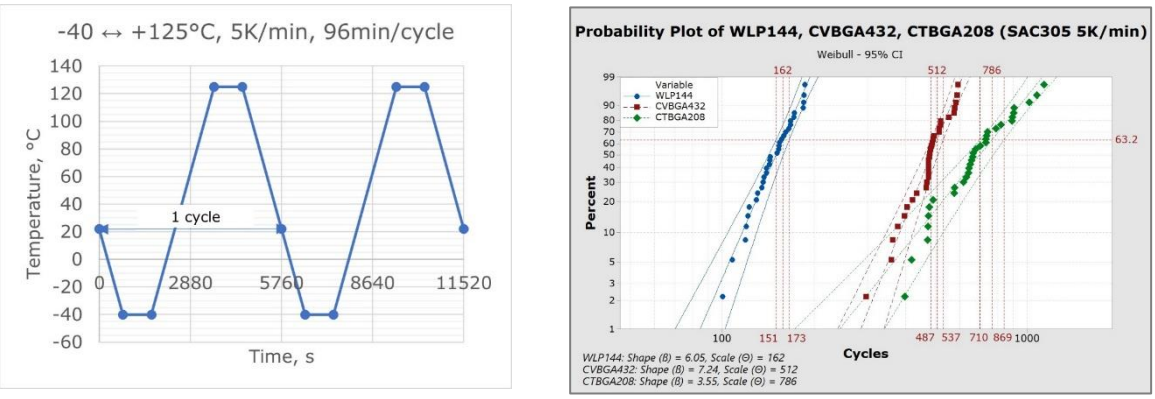

Figure 3 The thermal cycling test condition used in the BLR tests (left). The probability plot of the WLP144, CVBGA432 and CTBGA208 failure (right).

Parameter	Unit	WLP144	CVBGA432	CTBGA208
Engelmaier Input Parameters				
t_D	min	15	15	15
L	mm	5.96	13.00	15.00
W	mm	5.96	13.00	15.00
h	mm	0.19	0.18	0.28
α_C	1/°C	2.60e-6	5.85e-6	8.18e-6
α_S	1/°C	1.52e-5	1.52e-5	1.52e-5
Engelmaier Calculated Parameters				
c (10)	-	-0.452	-0.452	-0.452
L_D (11)	mm	4.21	9.19	10.61
$\Delta\alpha$	1/°C	1.26e-5	9.35e-6	7.02e-6
Engelmaier Output Parameters				
$\Delta\gamma$ (9)	-	0.0457	0.0789	0.0444
$N_{f(50\%)}$ (8)	**cycles**	**324**	**96**	**344**

Table 3 Engelmaier model input and output parameters [17].

Under the theoretical approach, we first determine the fatigue life of the parts using the analytical Engelmaier model, as in Table 3. We also use the Ansys Sherlock tool, which determines the shear strain with a modified Engelmaier equation, as in Table 4. Further, we use FEA to determine the failure criteria and the fatigue life of the parts. Figure 4 shows the geometry of the WLP144 with a focus on the solder joint, and Figure 5 shows the corresponding mesh. We created a similar model for the other two parts, then assembled the independent component models in the test PCB model, as in Figure 6. In [18], [19] and [20], we discussed PCB modeling approaches and material calibration and guidelines for reliability assessment. Lastly, as in Figure 7, we constrained the PCBFigure 7 to allow for free expansion during thermal cycling.

Parameter	Unit	WLP144	CVBGA432	CTBGA208
σ	MPa	71.31	58.88	39.81
ΔW	mJ/mm^3	2.831	3.078	1.317
$\Delta\gamma$	-	0.0397	0.0523	0.0331
$N_{f(63\%)}$	**cycles**	**186**	**171**	**400**

Table 4 Ansys Sherlock Solder Fatigue Outputs.

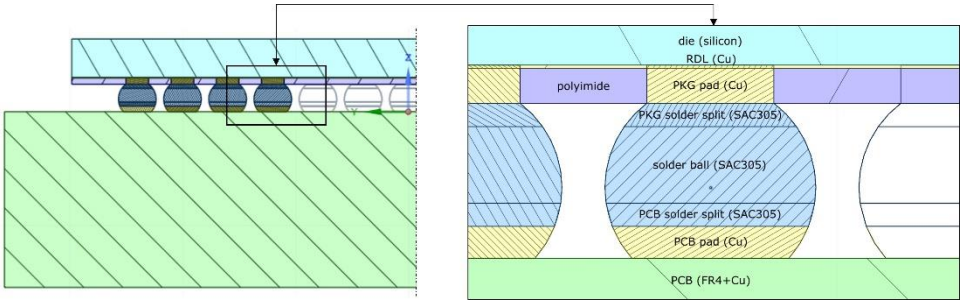

Figure 4 WLP144 cross-section view detail. Images used courtesy of ANSYS, Inc.

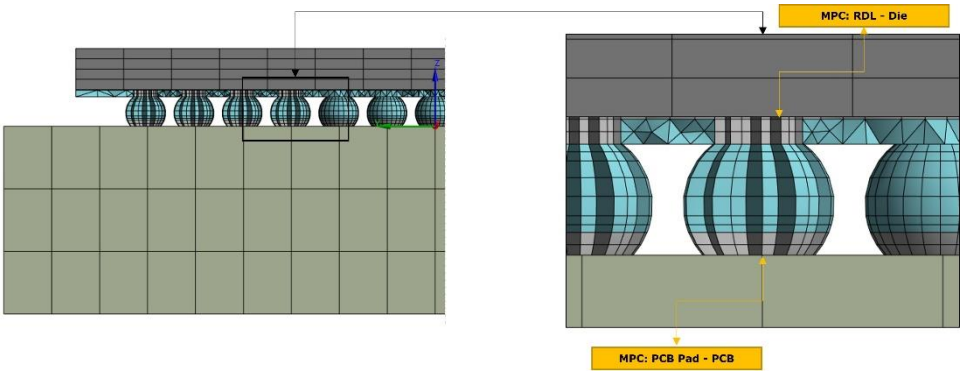

Figure 5 WLP144 mesh cross-section view detail. Images used courtesy of ANSYS, Inc.

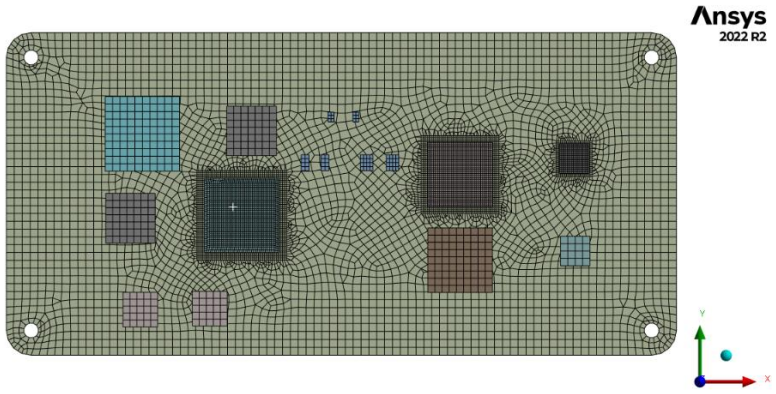

Figure 6 Assembly mesh. Image used courtesy of ANSYS, Inc.

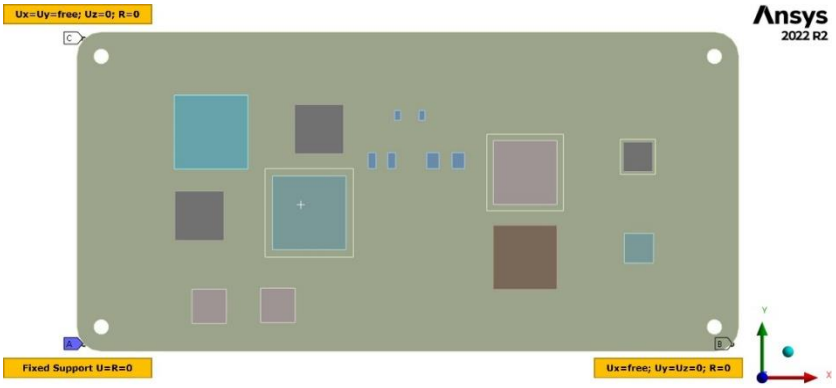

Figure 7 BLR boundary conditions. Image used courtesy of ANSYS, Inc.

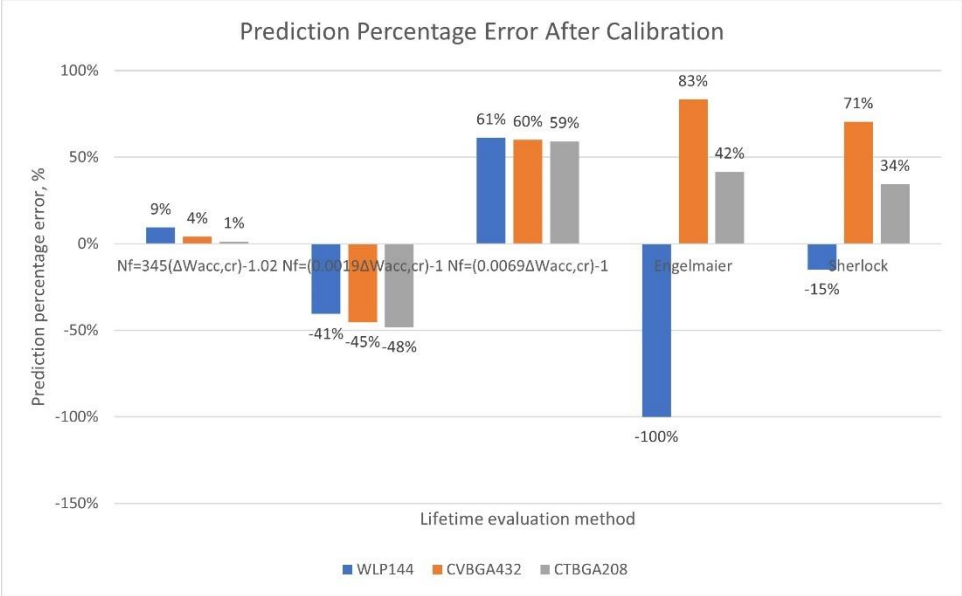

Figure 8 BLR prediction percentage error to test result after calibration.

For the CVBGA432 and CTBGA208, we assumed both to have the same generic substrate. We aim thus to calibrate the substrate material to get better life estimations. For CTBGA208, we had to increase the substrate's E and CTE to decrease the creep deformation in the solder joints. For the CVBGA432, we need to increase the failure criteria. By reducing the substrate modulus and CTE, we increase the error to 71% for the Sherlock prediction. However, in the FEA, the failure criteria increase, leading to a predicted lifetime within 4% of the test result. After calibration, the Schubert model underpredicts the parts' lifetime by up to 9%, while Syed overpredicts the lifetime by 41-48%, and the revisited Syed underpredicts the lifetime within 59-61%, as in Figure 8.

The main effect that a system integration brings is the PCBA-constrained deformation due to its fixations. To emulate system-level effects, we fix the four holes of the PCBA and re-solve the model without any other changes. In the fixed PCB, the WLP144 would fail first, followed by the CTBGA208 and CVBGA432. However, according to all prediction methods except for Syed, the WLP144 lasts longer in the SLR setup, while the other two parts would present failures earlier in SLR than in BLR, as in Figure 9.

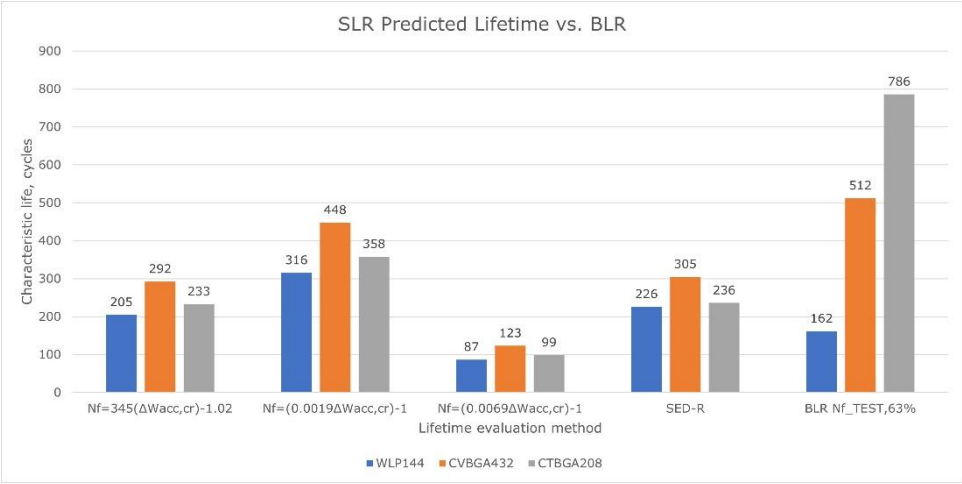

Figure 9 SLR vs. BLR characteristic life evaluation by the different methods considered.

Following the board-level reliability assessment and calibration, we attempted an evaluation of the parts' reliability under simplified system-level boundary conditions. Pursuing the research presented in this chapter and PCBA modeling studies in the published papers in Figure 10, we propose a simulation workflow for PCBA low-cycle fatigue assessment.

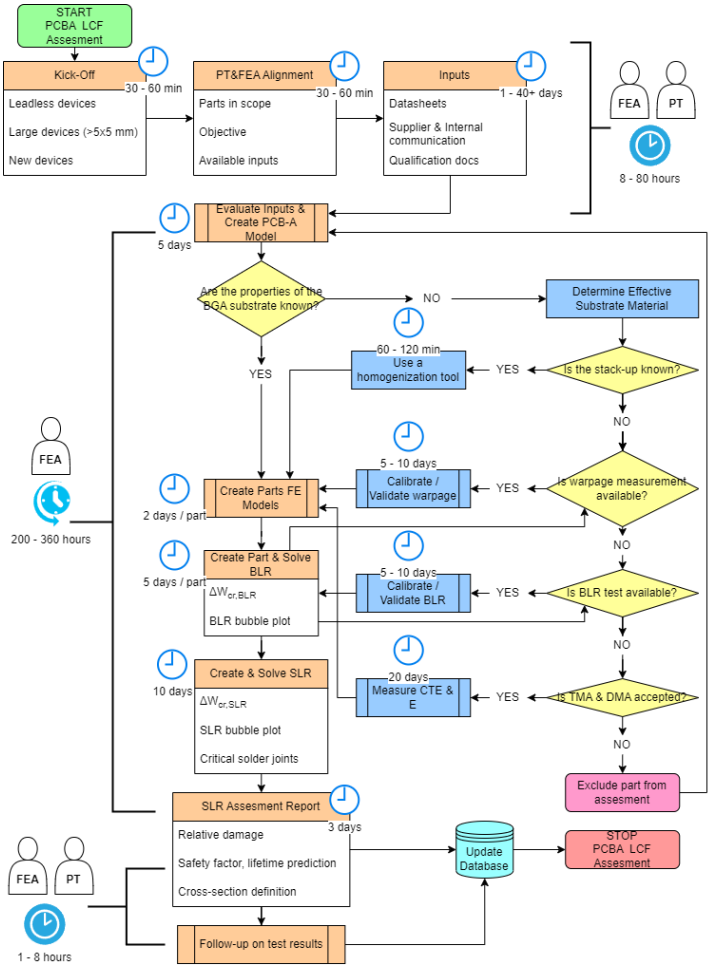

Figure 10 Proposed PCBA low-cycle fatigue assessment workflow showing all necessary steps and resources. Image used courtesy of Continental AG.

The first part of the research program (2017-2020) focused on independent study, networking, testing and review of tools and methods, which resulted in an early proposal of the discussed workflow. Next, the implementation of the proposed workflow spanned three years in different stages:

- Build knowledge and competence through corporate worldwide solder joint reliability learning sessions (2020) with 67 participants from ten departments, corporate technical hours (2021), cross-department one-to-one training and support on tools and methods (2021-2022), and regular user group meetings (2022-2023).

- Coordinate and lead solder fatigue simulations in a global team of ten structural analysis engineers, one-to-one training, and support (2020-2023).

- Implement the workflow on more than 70 parts on 17 product designs, focusing on providing clear outputs, such as the risk of failing the design validation test and cross-section definition (2020-2023).

Following implementation, the standardization phase took place in late 2022 as in the form of a predictive reliability assessment process, including process training, step-by-step tutorials, supervision of ongoing tasks and predictive reliability assessment technical hour for non-specialized audiences. We could correlate 21 parts in the validation phase with the physical test outcome in Figure 11. We created a grading system, as in Table 5, to compare the simulation outputs to the test outcomes. The fatigue analysis correctly identified the failure risk for 17 parts, underestimated the risk for two FCBGAs, one lead frame BGA and did not include one BGA.

Simulation Criteria	**Test Criteria**	**Grade**
Low (D<3 or SF>5)	minor crack <25% or pass	1
Medium (3≤D≤5 or 1≤SF≤1.5)	large crack 25-95% or pass	2
High (D>5 or SF<1)	full crack >95% or fail	3

Table 5 Grading system for simulation vs. test comparison. D stands for relative damage, and SF for the safety factor.

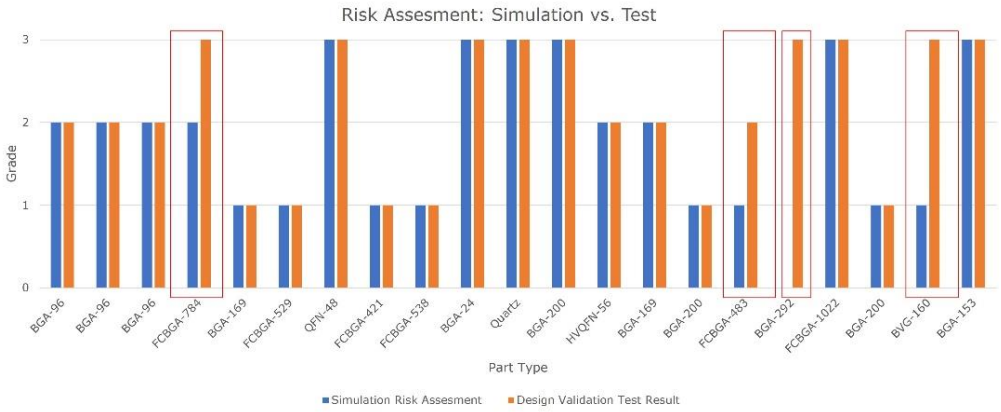

Figure 11 Validation of the proposed workflow: simulation vs. test risk assessment. Image used courtesy of Continental AG.

4 Discussion

The research findings indicate that board-level analysis, whether analytical or numerical, can be employed to optimize specific aspects such as the coefficient of thermal expansion (CTE) or elastic modulus (E). In evaluating the stress state in solder joints at the system level, our research findings suggest that the most suitable approach is to directly integrate a detailed board-level reliability (BLR) model into the printed circuit board assembly (PCBA) within the system model. This method ensures consistency over time and across different users, as demonstrated in the system-level reliability assessment conducted in our study. Focusing on the desired outcome is essential when choosing the appropriate simplifications for the system-level reliability assessment. Our research culminated in developing a simulation workflow for system-level reliability assessment, the foundation for a company-wide simulation process. While statistical validation of the outputs was not part of the research program, we conducted validation by applying the methods discussed in this thesis to over 70 parts across 17 different product designs. The results demonstrated a favorable outcome in terms of risk assessment when compared to test results.

5 Conclusion

The research addressed a practical problem in the automotive parts manufacturing industry by providing practical guidelines for predictive reliability assessment. The findings have real-world applications in selecting materials and components, optimizing mechanical designs, implementing redundancy, defining cross-section analysis, and proposing reliability enhancement measures. These guidelines serve as valuable tools for automotive manufacturers to enhance the reliability of their products, ensuring better performance and reducing the risk of failures in critical components.

The research outlook focuses on several critical areas for further exploration and development. These include automatizing processes and building a comprehensive database for materials and components. Potential areas of interest are simulating very large arrays and using design of experiments (DoE) to determine system-level effects.

The research contributions can be summarized as follows:

- PCB Modeling: The research papers [18], [19], and [20] explored various aspects of PCB design and analyzed the impact of factors such as mechanical properties, geometries, and material choices on the reliability of the PCB.
- System-Level Modeling: In [11] and [16], the research focused on system-level modeling by integrating detailed board-level models into the system model to analyze the reliability of the entire electronic system.
- Experimental Data, Analytical Calculations, Numerical Simulations: the thesis and [17] combine experimental data, analytical calculations, and numerical simulations. These research contributions showcased the use of different methodologies to validate and refine reliability assessments.
- System-Level Approach, Workflow, Proposed Tools & Methods: The thesis proposed a system-level approach to reliability assessment and developed a comprehensive workflow. It introduced tools and methods to streamline the analysis process, ensuring consistency and efficiency in reliability evaluations. These contributions provided a structured framework for conducting system-level reliability assessments.
- Proving the Influence of System-Level Effects on Part Reliability: The research demonstrated the impact of system-level effects on part reliability. Considering the interactions and dependencies between components, the research shows that system-level factors can significantly influence the reliability of individual parts.
- Competence Building and Knowledge Sharing: The research aimed to build competence through coaching, dissemination, work groups, and company-wide implementation.
- Simulation Process and Automatization Scripts: The research developed a simulation process and automatization scripts to streamline reliability assessments. These contributions improved the efficiency of the analysis process, reducing manual effort and increasing productivity. Training materials and a part and material database were also developed, further supporting the simulation process.

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