CONTRIBUTIONS TO THE REDUCTION OF THE ACOUSTIC NOISE GENERATED BY MULTILAYER CERAMIC CAPACITORS IN AUTOMOTIVE ELECTRONIC MODULES

PhD Thesis – Summary

for obtaining the scientific title of doctor at

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author Eng. Corina-Nicoleta COVACI (married Vidoni)

scientific coordinator Univ.prof.dr.eng. Aurel GONTEAN

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I developed this Ph.D. thesis during my work in the Applied Electronics Department of the University Politehnica Timișoara. The thesis is structured in seven chapters, followed by annexes and bibliography. Statistically, the thesis is characterized by:

- A total number of 165 pages, including 119 in the thesis and 46 pages in the annexes and bibliography
- 100 figures in the thesis and 30 figures in the annexes
- 11 tables in the thesis and 8 tables in the annexes
- 72 literature references

Chapter 1 – Introduction

In the first chapter, I present the motivation for choosing the research theme, the importance, the novelty, and the actuality of the subject, the research hypothesis formulation, and the thesis structure.

Motivation for choosing the research theme

Multilayer ceramic capacitors are passive components, indispensable in modern electronic devices, whose dielectric is usually made of barium titanate (BaTiO3). The two main electromechanical properties of barium titanate, piezoelectricity, and electrostriction, cause an acoustic noise generated by the vibration of the MLCC's inner electrodes in the presence of an electric field. This phenomenon is known in the literature as "singing capacitors".

We should understand that, even if the ceramic capacitors are the main reason for the singing capacitor phenomenon, the capacitors' vibration has a resonance frequency in the order of megahertz. Therefore, this vibration does not represent an issue itself. The singing capacitor phenomenon appears in the moment when the capacitors' inner electrodes are transferred to the PCB, and it starts to vibrate with the resonance frequency in the audible domain of 20Hz – 20kHz.

Therefore, the singing capacitor phenomenon is interdisciplinary, and it must be analyzed from an acoustic, mechanical, and electrical point of view. From an electrical point of view, the inner electrodes' vibration is caused by an electric field applied to the capacitors (the piezoelectric and electrostrictive effects of the dielectric material). The inner electrodes' vibration is transferred through capacitors terminals to the PCB, which starts to deform, transforming the issue into a mechanical one. If the PCB vibration has a resonance frequency within the 20Hz-20kHz domain, the phenomenon must be studied also from the acoustic point of view.

Importance, novelty, and the actuality of the subject

The described phenomenon has recently appeared since the commercially available capacitors must have high capacitance in a small package. Due to the subject novelty, the main inconvenience of the acoustic noise caused by the ceramic capacitors is the lack of information available. There are few references for the singing capacitors phenomenon in the literature, and it is mentioned by a small number of electronic components manufacturers.

Although the phenomenon is not completely understood, and the research on the acoustic noise caused by ceramic capacitors has only recently started, it appears more frequent in electronic devices. Most of the time, the problem appears in the domains where the device is used nearby the user. This happens because the acoustic noise caused by the multilayer ceramic capacitors does not provoke functionality problems, it is only inconvenient for the device user. However, the presence of the singing capacitor phenomenon must be avoided since the user discomfort is considered a sign of low-quality product. In conclusion, there is a major interest in this subject, in the international context, due to the high number of electronic devices where the singing capacitor phenomenon can be present and its negative effect on the user experience.

Research hypothesis formulation

The scientific objective in this research is the presentation of the simulation methods and the experimental results for the singing capacitors phenomenon which appears in an electronic control unit developed by Continental Automotive™. The problem appeared from a practical necessity, I started with the phenomenon analysis, followed by a vibration analysis of the electronic system, the simulation results were validated by experiments, then followed by a series of additional experiments, where multiple methods for acoustic noise elimination or reduction were presented.

In the device development phase, the acoustic noise caused by ceramic capacitors can be prevented by simulating the electromechanical behavior. In the literature, the most known electromechanical simulations are modal analysis and harmonic analysis. While modal analysis studies the intrinsic vibration of the PCB, harmonic analysis studies the capacitor vibration effect on the PCB behavior. So, when studying the device behavior using a harmonic analysis in the development phase, we can avoid placing the multilayer ceramic capacitors in critical areas.

When the product has a higher development phase when we discover the singing capacitors phenomenon presence, design modifications are not allowed. In this case, the solution could be changing the capacitor technology. This solution affects the cost, but in most cases, this solution is cheaper compared with the design modifications cost.

Besides the simulation methods and solutions to reduce the singing capacitor phenomenon, the literature offers information related to the direct and indirect measurement of the acoustic noise caused by multilayer ceramic capacitors.

Given the structure and approach, this thesis is an applicative research of the singing capacitor phenomenon. I started with a practical issue, where I analyzed the phenomenon, then I modeled and simulated the device. The simulation results were validated and afterwards, I proposed several efficient methods to eliminate or reduce the acoustic noise caused by the multilayer ceramic capacitors.

Thesis structure

The first chapter presents the motivation for choosing the research theme, followed by an introduction about the importance, novelty, and the actuality of subject. The chapter ends with the research hypothesis formulation and thesis structure.

The second chapter presents the state of the art. In this chapter, I analyze the literature research about the singing capacitor phenomenon, measurement methods, solutions to eliminate or attenuate the acoustic noise caused by multilayer ceramic capacitors, and prevention methods.

In chapter three, I presented a detailed analysis of the problem, where the case study is presented, and the first measurements are made.

Chapter four is the simulation chapter. This chapter contains a theoretical introduction to the modal and harmonic analysis, followed by the modal and harmonic analysis of the system presented in chapter three. After the results interpretation, I propose two solutions to attenuate the singing capacitors phenomenon. The first proposal focuses on the mechanical tension attenuation on the capacitors, while the second proposal focuses on the layout optimization by placing the capacitors in mirror geometric configuration. Both solutions are simulated using harmonic analysis, and the results are compared at the end of the chapter.

Chapter five validates the simulation results for mechanical tension attenuation on the capacitor and layout optimization solutions. The chapter ends with a comparative analysis of the original system, presented in chapter three, and the two solution proposals, taking into consideration both simulation and experimental results.

In chapter six, I presented additional alternatives investigated to reduce the singing capacitor phenomenon. These alternatives are divided into four categories: solutions focused on fabrication process modifications (placing the capacitors in a vertical orientation, solder paste reduction, oven curing, varnishing, and potting), solutions focused on component modifications (using C0G dielectric capacitors), solutions focused on noise muffling (using anti-vibration grommets or EPDM foam) and alternative solutions for layout optimization (by placing the capacitors in parallel geometric configuration).

In the last chapter, I present the original contributions summary, the scientific publications list during the research, and the research conclusions.

Chapter 2 – State of the art

Multilayer ceramic capacitors (MLCC) are passive components indispensable to modern electronic devices. They are composed of three main elements: inner electrodes, outer electrodes, and dielectric material. Their popularity is due to the multiple advantages they present, such as small dimensions and price, favorable electric characteristics (e.g., small equivalent series inductance, small equivalent series resistance, good frequency response), and their ability to be used for long periods at high temperature or in high voltage applications.

These advantages are due to the high permitivity material the most dielectrics are made of – barium titanate ($BaTiO_3$). Despite the barium titanate advantages, its electromechanical properties (piezoelectricity and electrostriction) cause one of the newest electronic devices problem: the acoustic noise caused by multilayer ceramic capacitors, known in the literature as singing capacitor phenomenon.

Due to the piezoelectricity and electrostriction presence, when an electric field is applied to the capacitor, its inner electrodes start to vibrate. This behavior is described in equation (2.9), which was used to model the multilayer ceramic capacitor behavior.

$$s_z = \left(d_{33}E_{DC} + M_{33}E_{DC}^2 + \frac{1}{2}M_{33}E_{AC}^2\right) + (d_{33} + 2M_{33}E_{DC})E_{AC}\cos\omega + \frac{1}{2}M_{33}E_{AC}^2\cos 2\omega t \qquad (2.9)$$

where s_z is the mechanical tension, d_{33} is the piezoelectric coefficient M_{33} is the electrostrictive coefficient, E_{DC} is the continuous component of the applied electric field, E_{AC} is the alternative component of the applied electric field, and ω is the angular frequency.

The resonance frequency of the MLCC vibration is in the MHz order. Therefore, it is not heard by the human ear. However, since the MLCCs are SMD (Surface-Mount Device) components, the induced vibration is transferred to the PCB (Printed Circuit Board) through the solder joint. When an alternative voltage is applied to the capacitor, the dielectric material extends in the applied field direction, causing the PCB deformation, as presented in Fig.2.2. Hence, the PCB starts to vibrate, and vibration frequency can reach the audible range of 20Hz-20kHz. In this case, the singing capacitor phenomenon appears.

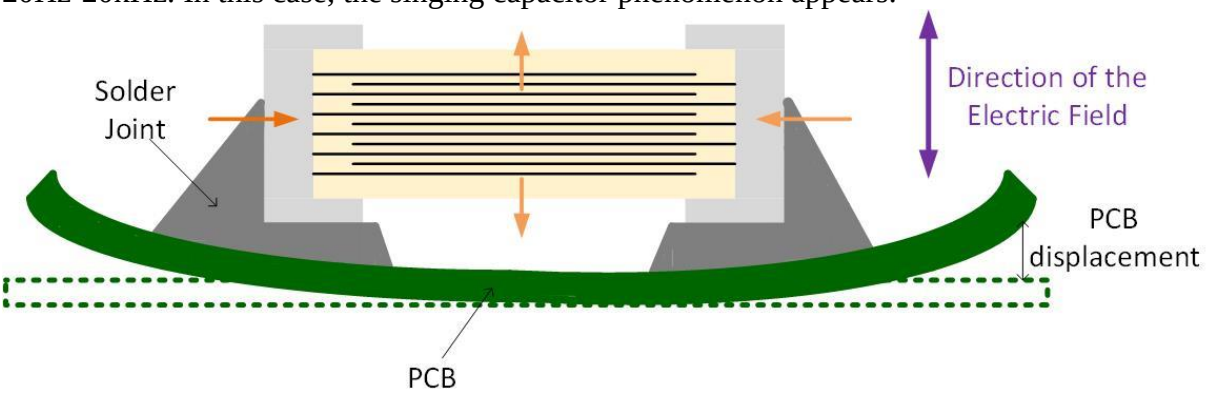


Fig.2.2. Vibration transfed from the electrods to the PCB

The singing capacitor phenomenon can be measured by acoustic noise or vibration measurement.

For acoustic noise measurement, the most used method is the SPL (Sound Pressure Level) measurement, defined in equation (2.11):

$$SPL = 20\log\left(\frac{P_{RMS}}{P_0}\right) \qquad (2.11)$$

where P_{RMS} is the Root Mean Square of the pressure deviation from the atmospheric pressure, and P_0 is the reference level.

Usually, this investigation requires a microphone, an FFT (Fast Fourier Transform) analyzer, and an anechoic box or room. The microphone has two sensors: one pressure sensor, used to measure the sound pressure in the air, and a speed pressure sensor, used to measure the air movement speed. The FFT analyzer is used to obtain the SPL spectrum, and the anechoic box is used to reduce the external acoustic noise, which could influence the measurement results. The most used method to measure the vibration is PCB scanning using LDV (Laser Doppler Vibrometer) equipment. This equipment detects the Doppler displacement of the reflected light to measure the surface vibration without contact. The LDV has a submillimeter domain resolution. Therefore, it is suitable to measure the small-dimensioned MLCCs. Other vibration measurement methods are the optical fiber sensor, piezoelectric accelerometer, active simulation method, and vibration and voltage coherence method. These are rarely used in the literature.
In the literature, there is a multitude of solutions for the singing capacitor phenomenon, among which are the usage of alternative capacitors, placing the MLCC in a certain orientation or a specific area of the PCB, the solder paste reduction, etc. Moreover, the capacitors suppliers are aware of this new electronic issue and propose several commercial solutions (e.g., metal terminal capacitors, interposer capacitors, thicker dielectric layer capacitors, aluminum substrate capacitors, metal plate capacitors and dipped radial leads capacitors) to attenuate or reduce the acoustic noise caused by MLCCs.
Also, in the literature are recommended different geometric configurations to place the capacitors, depending on the type of capacitor used. These configurations are “L” or “T” shaped, parallel, or mirror. Also, the acoustic noise attenuation efficiency depends on the signals applied to the capacitors (in phase or out of phase signals), as shown in Table 2.2.

Capacitor type	**Applied signals**	**„L” or „T” shape configuration**	**Parallel Configuration**	**Mirror Configuration**
Regular capacitor	In phase	NO	NO	YES
	Out of phase	NO	YES	NO
3-terminal capacitor	In phase	YES	NO	NO
	Out of phase	NO	YES	NO
Reverse geometry capacitor	In phase	NO	NO	YES
	Out of phase	NO	YES	NO
Interposer capacitor	In phase	NO	NO	YES
	Out of phase	YES	YES	NO

Table 2.1. Efficiency for differenent layout configurations depending on the type of capacitor used
* The table contains the answer to the question “Is this combination effective?”

Therefore, when using the regular capacitor, the parallel configuration is the most suitable one when the applied signals are out of phase. Otherwise, it is recommended to use the mirror configuration.
In the literature, for prevention, it is recommended the modal analysis, which describes the mathematical model of the dynamic behavior, and harmonic analysis, which describes and analyzes the phenomena with a recurring periodic character.

Chapter 3 – Detailed analysis of the issue

To study the singing capacitor phenomenon, I used an electronic device where the acoustic noise caused by the multilayer ceramic capacitors was observed. The equipment is an electronic control unit developed by Continental Automotive™ Corporation.
The LED Driver module, where the 2.2µF problematic capacitors are placed (C5, C6, C10, C11, C15, and C16 from Fig.3.1), commands the luminous intensity of multiple LED groups.

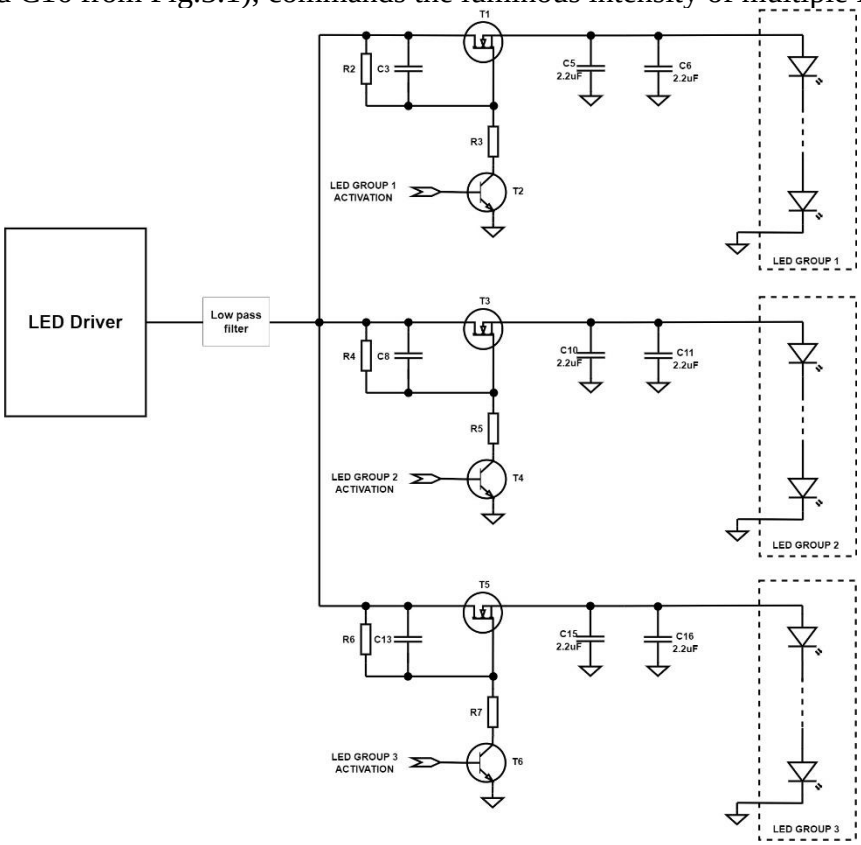


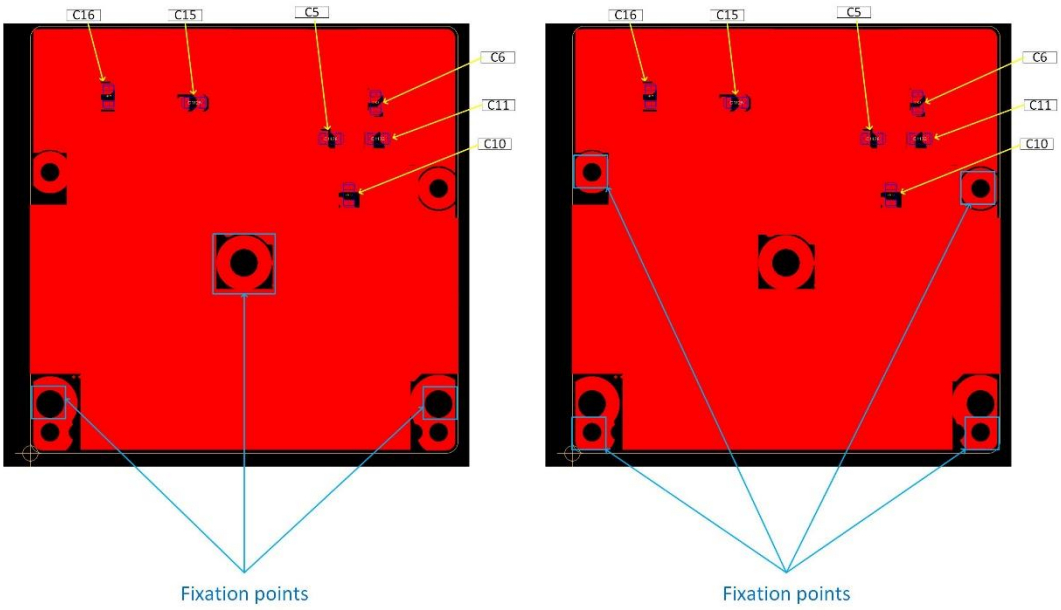
Fig.3.1. Electronic schematic of the studied module

The module behaves as a constant current source, which generates 4A pulses with a 470µs duration and a frequency of 35Hz. These pulses are used to power the infrared LED groups. For the LEDs used in our application, the voltage drop on every LED group is approximative 10V.
We used two command modes for the LED groups, which are presented in Table 3.1. The command modes are selected using the "LED GROUP 1 ACTIVATION", "LED GROUP 2 ACTIVATION" and "LED GROUP 3 ACTIVATION" signals.

LED command modes	**Description**
Command mode 1	The LED Driver powers only the LED group 1, while LED group 2 and 3 stay inactive
Command mode 2	The LED Driver powers one by one the LED groups, without having two LED groups active in the same time

Table 3.1. LED command modes

Also, the system has two fixation modes in the car. These fixation modes are described in Fig.3.2, together with the relative positions of the problematic capacitors.



a) b)

Fig.3.2. Fixation modes in the car: a) in three points; b) in four points

The PCB vibration for the three-point fixation (Fig.3.2.a) is more intense than the four-point fixation (Fig.3.2.b). Thus, the singing capacitor phenomenon is more pronounced when using the three-point fixation. Therefore, the experiments from this chapter are made using only the less favorable case - the three-point fixation mode.

As mentioned in Chapter 2, there are two main measurement methods for the singing capacitor phenomenon: vibration and acoustic measurements.

For vibration measurement, I used a piezoelectric accelerometer placed in the center of the PCB. The accelerometer I used is the 352A74 model, developed by PCB Piezoelectronics™. I measured the PCB vibration using the piezoelectric accelerometer for both LED command modes. The results for LED command one are presented in Fig.3.4. The results for LED command two are presented in Fig.3.5. The red waveform represents the information captured by the accelerometer, while the blue one represents the LED Driver's output voltage. Although we can analyze the vibration differences between the two measurements, this method does not offer quantitative information about the acoustic noise since the signal measured by the accelerometer is dependent on the temperature and the applied force when it is placed on the PCB. Since the piezoelectric accelerometer is manually placed in the PCB, there are no conditions for repeatability. However, it can be observed that the captured vibration is present only during the voltage pulse duration, and the 20V voltage spikes are present at the beginning of every pulse.

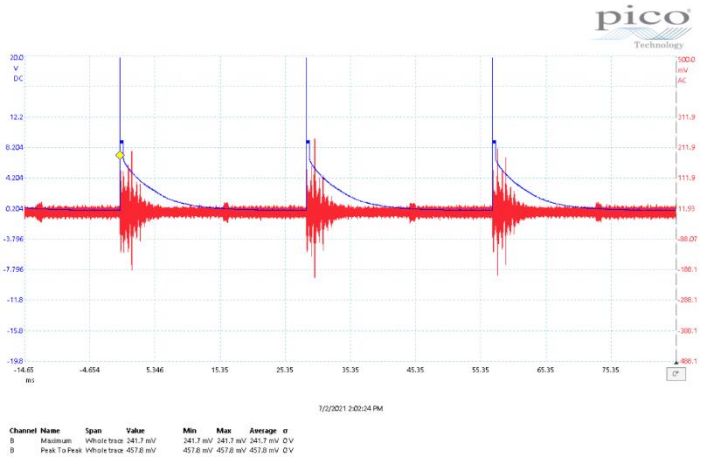


Fig.3.4. PCB vibration for LED command mode 1

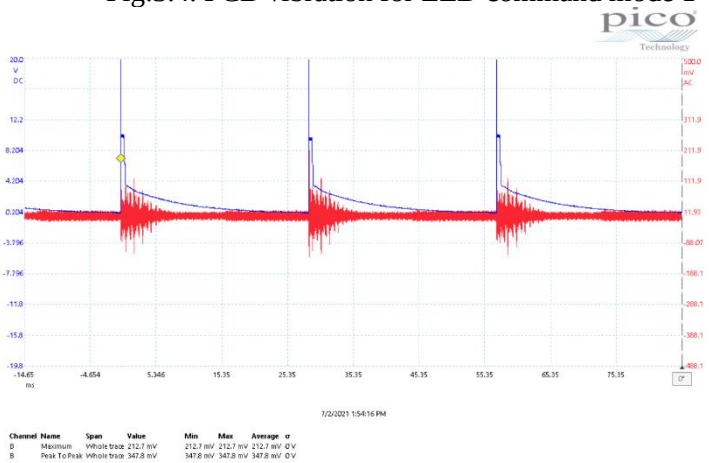


Fig.3.5. PCB vibration for LED command 2

To measure the acoustic noise caused by the multilayer ceramic capacitors, I used a microphone to measure the signal's SPL and Loudness. For better precision, the measurement was made in an anechoic room, where the acoustic noise is not reflected, and the external noises are not observed. The acoustic noise results are presented in Fig.3.8 – Fig.3.11.
For the four measurements, the system was functional for 10s, and then it was stopped for the next 10s to observe the difference between the measured acoustic noise and the anechoic chamber reference.

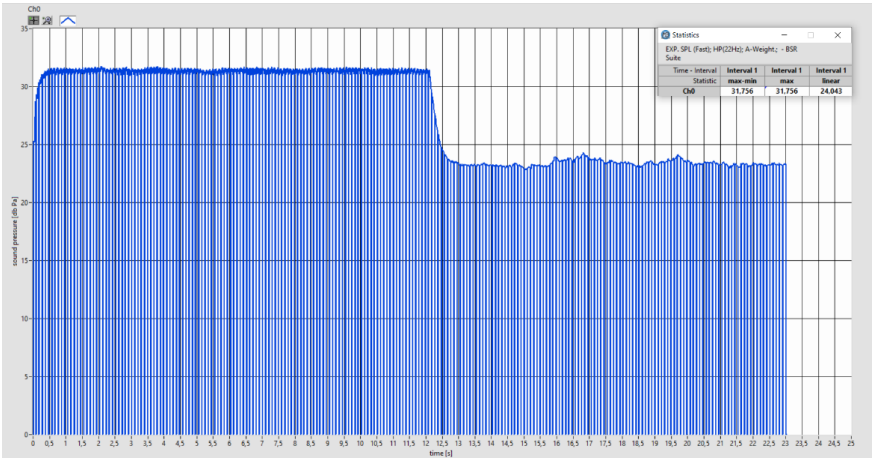


Fig.3.8. SPL measured for the LED command mode 1

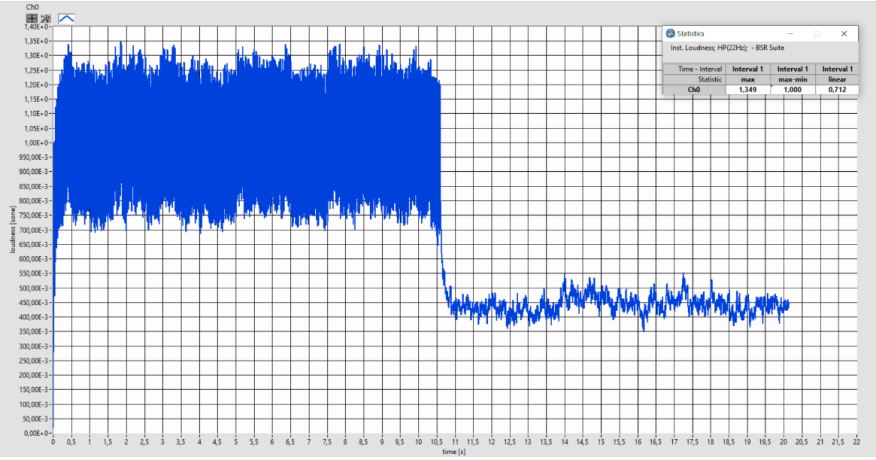


Fig.3.9. Loudness measured for the LED command 1

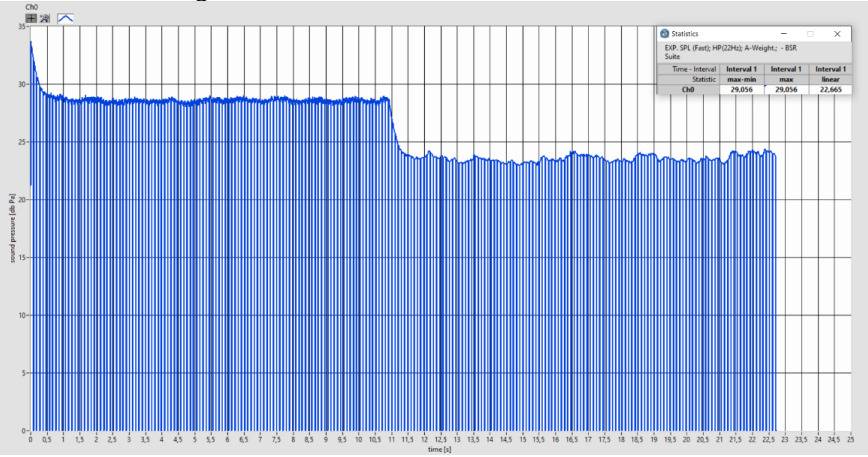


Fig.3.10. SPL measured for the LED command 2

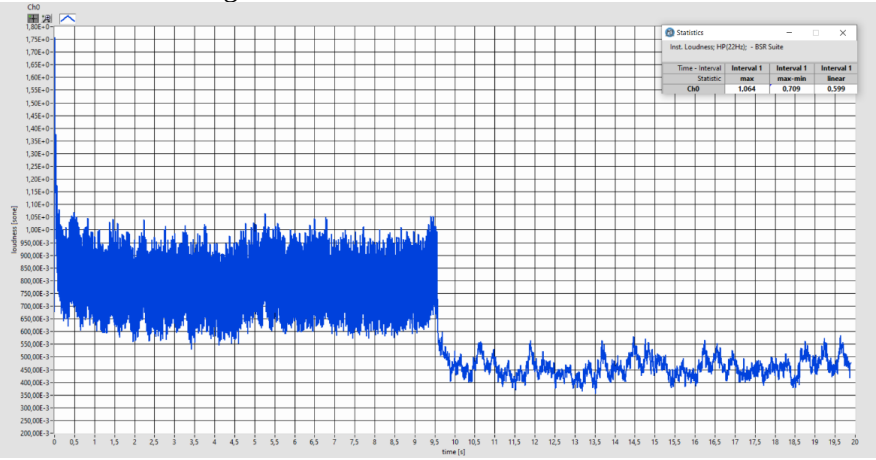


Fig.3.11. Loudness measured for the LED command 2

The initial acoustic measurement results are presented in Table 3.2.

Sound characterization method	**LED command mode 1**	**LED command mode 2**
SPL	31.75 dBPa	29.05 dBPa
Loudness	1.34 sone	1.06 sone

Tabel 3.2. The initial acoustic measurement results for the studied electronic sistem

Chapter 4 – Simulation

As mentioned in Chapter 3, the system has two fixation modes in the car: in three and in four points (described in Fig.3.2.). Since the acoustic noise caused by MLCC was observed only for the three-point fixation case, I made a modal analysis of the system to determine the modal shape differences between the two scenarios.

The analysis result is described in 30 modes, where the natural frequency and the theoretical maximum displacement for each mode are presented. In Fig.4.1 and Fig.4.2, the maximum displacement for each resonance frequency is represented for both four-point and three-point fixation.

For the four-point fixation, the maximum displacements are obtained in mode 23, at the frequency of 7427Hz, where the displacement is 1197µm, and in mode 15, at the frequency of 4627Hz, where the displacement is 1098µm. For the three-point fixation, the maximum displacements are obtained in mode 20, at the frequency of 6499Hz, where the displacement is1151µm, and at the frequency of 4581Hz, presented in mode 15, where we have a displacement of 982µm.

Since the obtained results are not better when we simulate one fixation mode or another, the modal analysis does not indicate why the system with four-point fixation is more silent than the system fixed in three points.

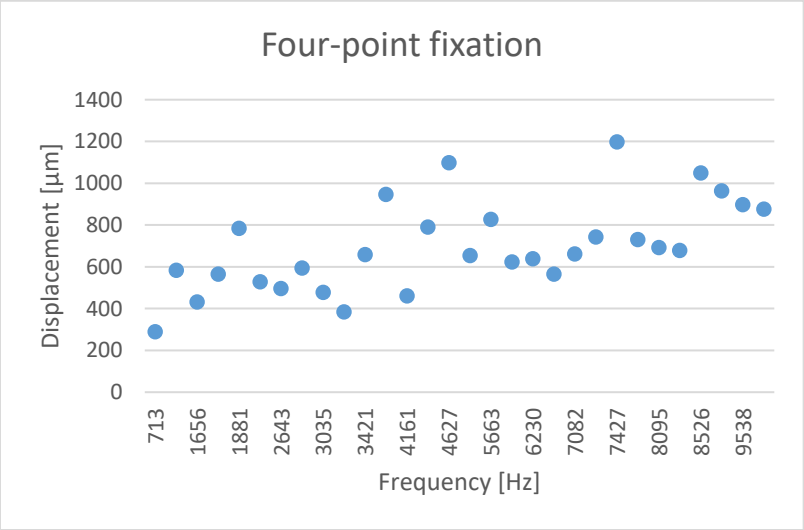


Fig.4.1. Modal analysis result – maximum displacement for four-point fixation

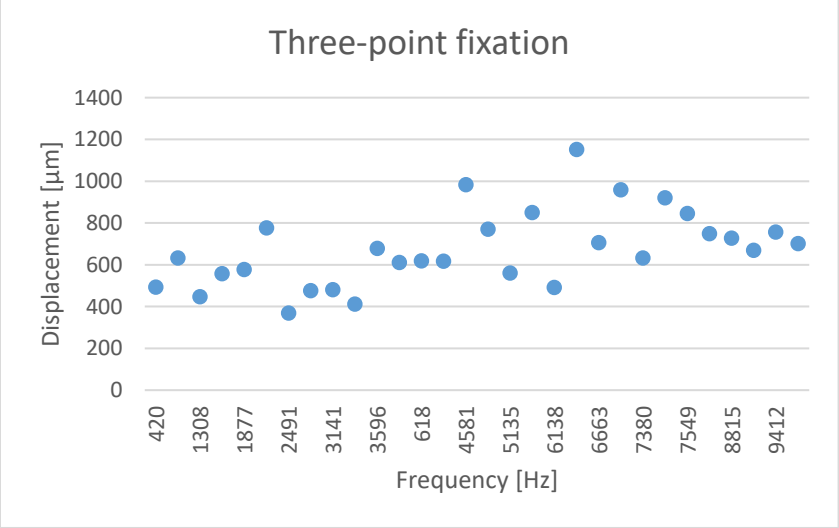


Fig.4.2. Modal analysis result – maximum displacement for three-point fixation

Next, I made a harmonic analysis of the system to determine the ceramic capacitor effect on the PCB vibration. For each fixation mode, the harmonic response was analyzed when a 2Pa force was applied to each problematic capacitor. The result contains 470 modes (presented in annexes), where the resonance frequencies are between 0Hz and 10kHz. In Fig.4.11, the harmonic response for the three-point fixation is presented, while the harmonic response for the four-point fixation is presented in Fig.4.12.
As we can observe, the four-point fixation is more favorable compared with the three-point fixation. As shown in Fig.4.11, the maximum displacement for the three-point fixation is 20.26nm at the resonance frequency of 407Hz, while in Fig.4.12, we can see a maximum displacement four times lower, 5.21nm at the resonance frequency of 788Hz, for the four-point fixation. When looking at the second harmonic, for the three-point fixation we observe a maximum displacement of 8.44nm at the resonance frequency of 613Hz, while for the four-point fixation, the maximum displacement is 1.49nm at the resonance frequency of 1.78kHz.

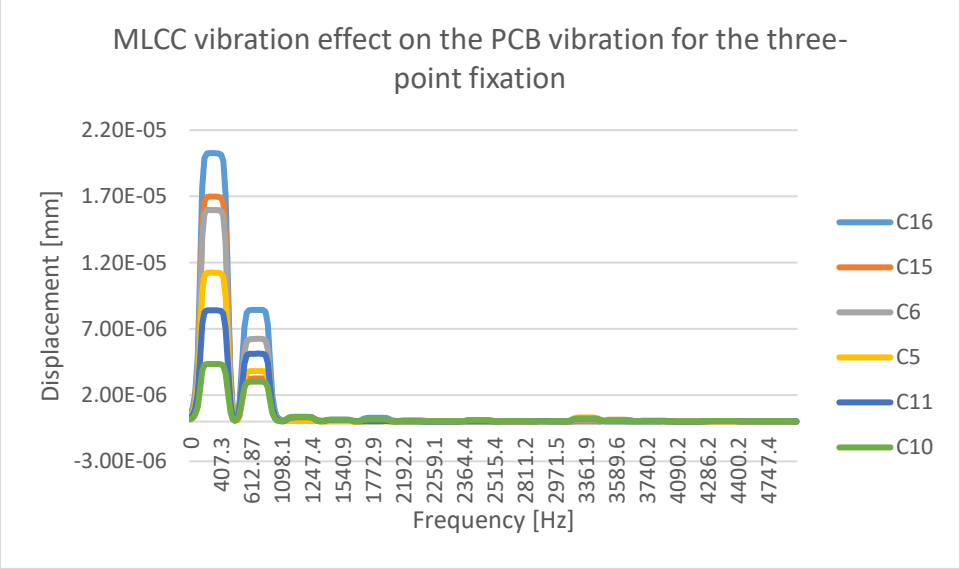


Fig.4.11. Harmonic response for three-point fixation

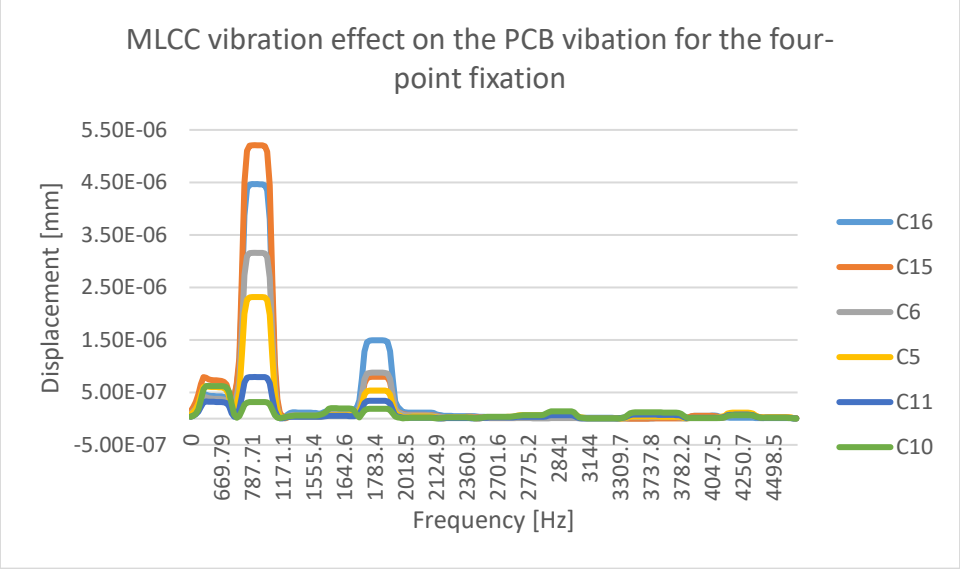


Fig.4.12. Harmonic response for four-point fixation

Another observation is that for the three-point fixation, the C16 capacitor effect has the most influence on the system vibration, for both fundamental and second harmonic, while, for the

four-point fixation, the fundamental is influenced mostly by the C15 capacitor, and the second harmonic is influenced mostly by the C16 capacitor.
Since the original results are available, I will describe two proposals for acoustic noise attenuation: mechanical tension attenuation on the capacitors and layout optimization.
In the last chapter, in Fig.3.4 and Fig.3.5, a 20V voltage spike can be observed at the LED Driver's output. This voltage spike is visible in every period, at the beginning of every pulse, causing additional stress on the MLCC.
After we analyzed the schematic, we determined that the voltage spike is generated by the C3, C8, and C13 capacitors, present in the delay circuits for every LED group (R2-C3, R4-C8, and R6-C13). These capacitors are charged before the activation of the MOSFET transistors T1, T3, and T5. Therefore, when one of the LED groups is activated, the corresponding MOSFET transistor is closed, and the delay capacitor is suddenly discharging, creating a voltage spike.
Since the delay is not necessary for the application, we removed the C3, C8, and C13 capacitors, as presented in Fig.4.17.

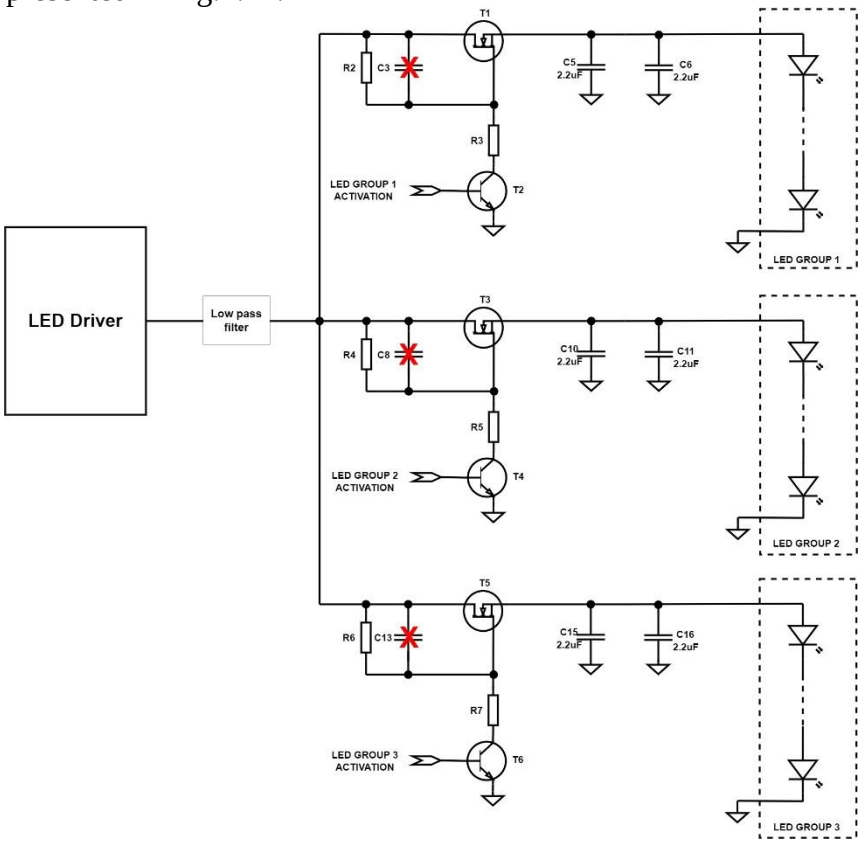


Fig.4.17. Electronic schematic for the voltge spike elimination

Besides this modification, the mechanical tension applied on the MLCCs can be reduced by pre-charging the capacitors/ To pre-charge the MLCCs, I added a voltage divider containing R7 and R8 resistors, placed at the LED Driver's output, as presented in Fig.4.18. When using this voltage divider, the voltage pulse generated by the LED Driver rises from the 5V level to 10V, in comparison with the original concept where the voltage pulse was rising from 0V level to 10V. Since the voltage difference is half the original, the piezoelectric and electrostrictive effects generate a smaller mechanical displacement.
In the harmonic analysis, the C3, C8, and C13 capacitors were not taken into consideration. Therefore, we can only analyze the effect of the pre-charged capacitors form the harmonic response point of view.

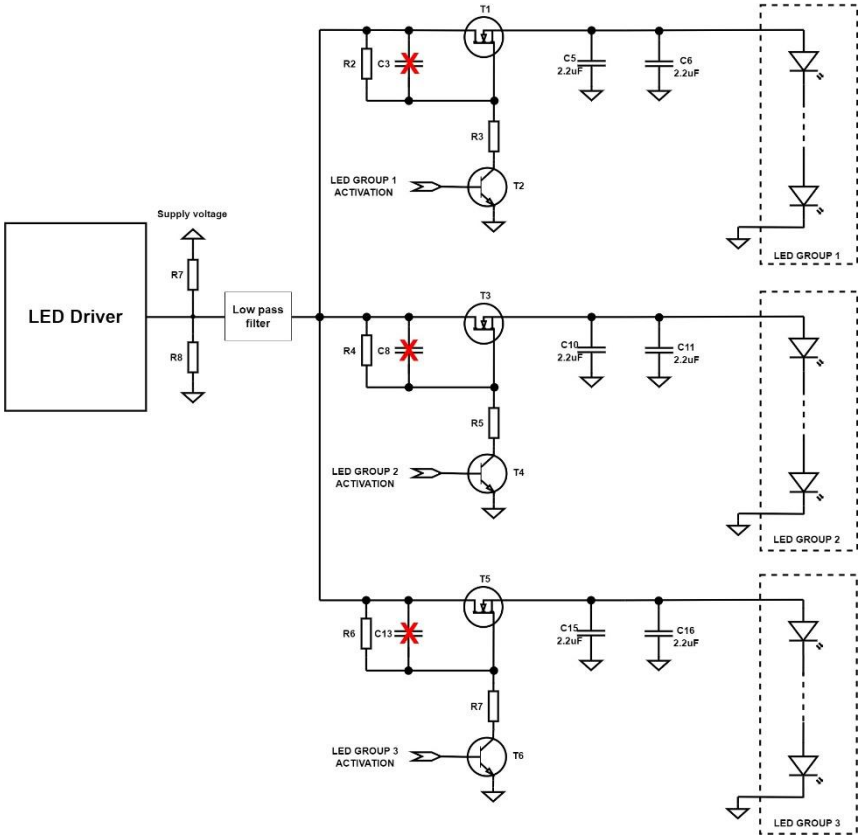


Fig.4.18. Electronic schematic for the pre-charged capacitors

For this harmonic analysis, I repeated the steps from the first simulation using the new layout, and I considered the force applied on the capacitors of 1Pa (half the force applied in the first analysis). The results are presented in Fig.4.19 and Fig.4.20, for both fixations.

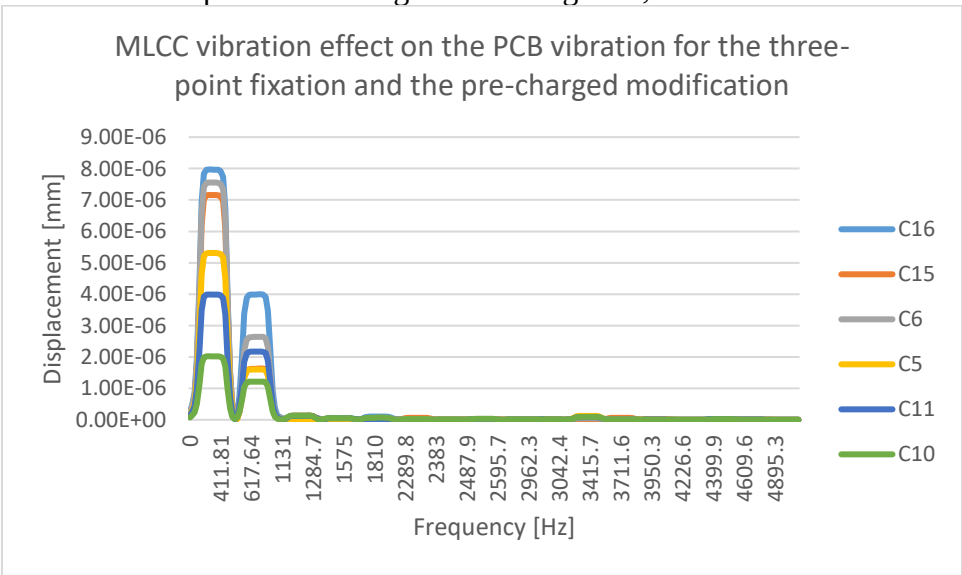


Fig.4.19. Harmonic response for the three-point fixation, for the pre-charged capacitors modification

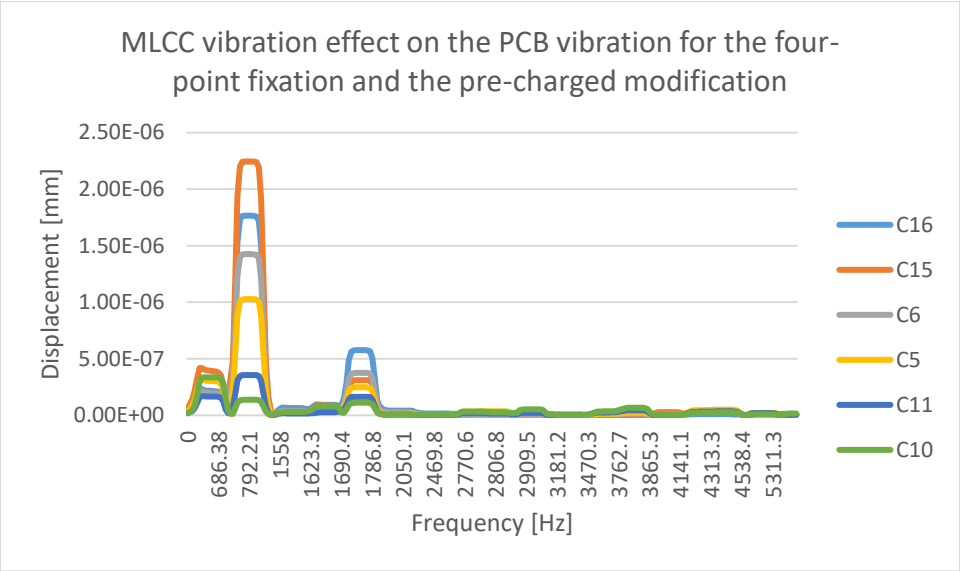


Fig.4.20. Harmonic response for the four-point fixation, for the pre-charged capacitors modification

A similarity can be seen between the behavior of the original and the improved design. For the three-point fixation, both the fundamental (which appears at the resonance frequency of 411Hz) and the second harmonic (which appears at 617Hz) are mostly influenced by the C16 capacitor. For the four-point fixation, the fundamental (which appears at 792Hz) is mostly influenced by the C15 capacitor, while the second harmonic (which appears at 1.77kHz) is mostly influenced by the C16 capacitor.

Although the resonance frequency values are similar to the first case, the displacement values are different. For the three-point fixation, we have a maximum displacement of 7.96nm (compared with 20.26nm in the first simulation), followed by a displacement of 3.99nm (compared with 8.44nm). For the four-point fixation, the maximum displacement is 2.25nm (compared with 5.21nm), and the second harmonic is 0.58nm (compared with 1.49nm). We can conclude that the simulation results present a reduced acoustic noise when the capacitors are pre-charged.

In Chapter 2, I presented the layout optimization solution for the singing capacitor phenomenon. As presented in Table 2.1, when we use regular capacitors, the parallel and mirror configurations are considered the most effective layout geometries in the literature. For the layout optimization of the series product, the mirror layout configuration, also known as back-to-back configuration, was chosen.

This modification started from the design of the pre-charged capacitor, where I replaced each of the 2.2µF capacitors with a pair of 1µF, placed in parallel, on different sides of the PCB. The package was also reduced from 1208 to 0805, as shown in Fig.4.25. These modifications are presented in Fig.4.25.

For this harmonic analysis, the force applied to the capacitors was also 1Pa, as in the previous simulation. Fig.4.26 and Fig.4.27 present the harmonic analysis results for the layout optimization modification.

Although in this case, we can observe multiple harmonics (compared with the previous analysis), the displacements are several orders of magnitude smaller. For the three-point fixation, we can observe a 117fm displacement, followed by an 80fm displacement. For the four-point fixation, the maximum displacements are 92fm ad 86fm.

Also, as shown in the previous cases, the left-side capacitors have the most influence on the PCB vibration, but the capacitors placed on the bottom side of the PCB create the maximum displacements.

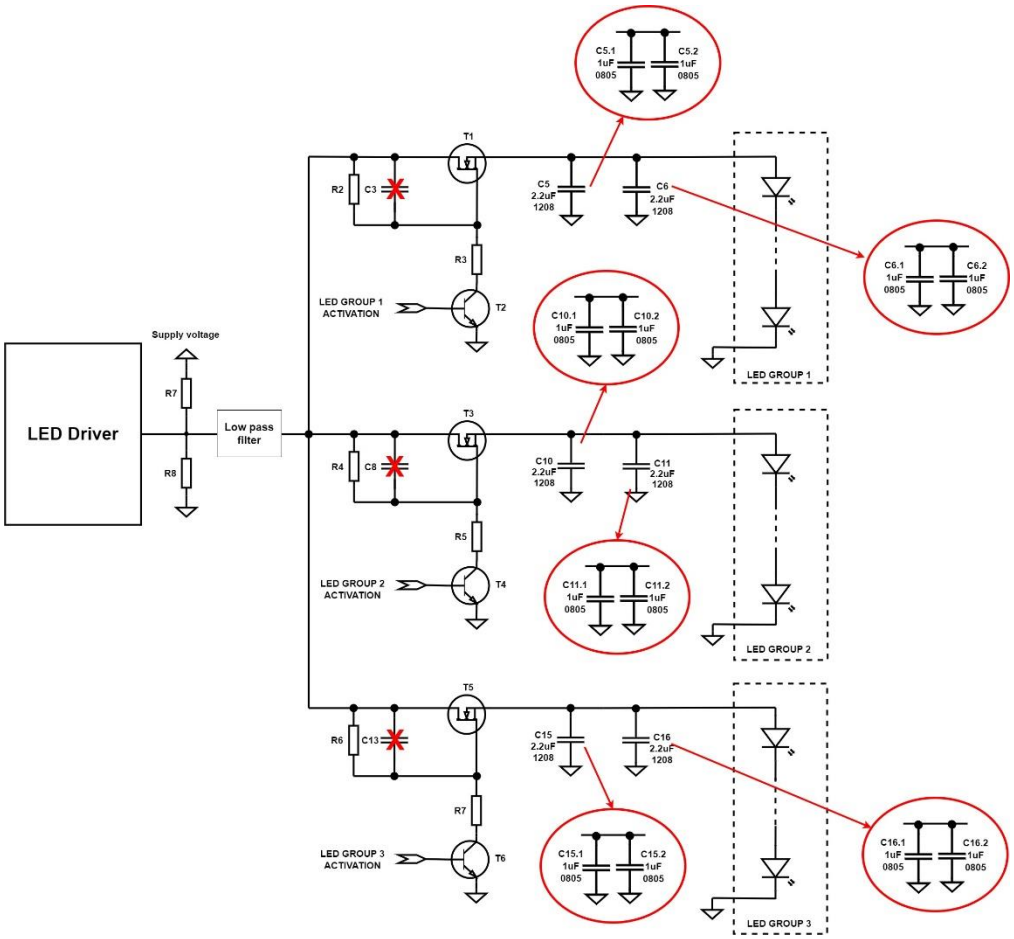


Fig.4.25. Electronic schematic for the layout optimization

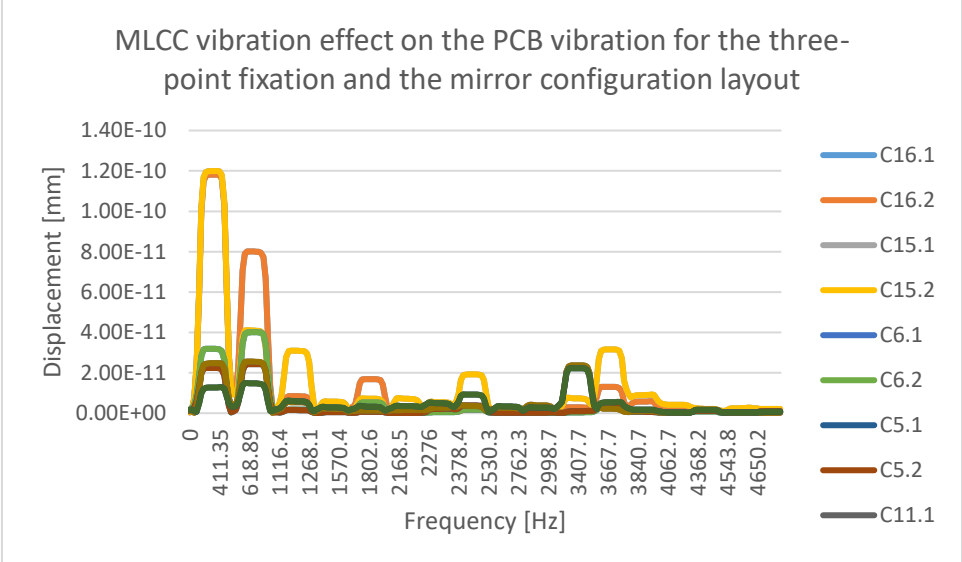


Fig.4.26. Harmonic response for the three-point fixation, for the layout optimization modification

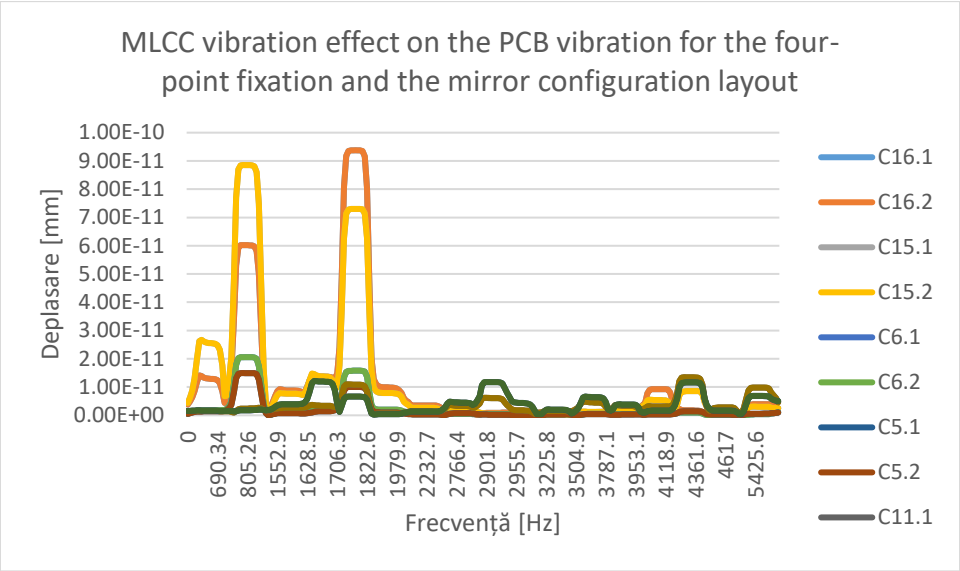


Fig.4.27. Harmonic response for the four-point fixation, for the layout optimization modification

Table 4.2 presents the maximum two values for the PCB displacement for every case investigated using the harmonic analysis.

Case investigated	Fixation mode	Fundamental magnitude	Second harmonic magnitude
Original design	In three point	20.26 nm	8.44 nm
	In four point	5.21 nm	1.49 nm
Pre-charged capacitors design	In three point	7.96 nm	3.99 nm
	In four point	2.25 nm	0.58 nm
Layout optimization design	In three point	117 fm	80 fm
	In four point	92 fm	86 fm

Tabel 4.2. Harmonic analysis results

The simulation results suggest an acoustic noise improvement from one modification to another. In the following chapter, I will validate these results using experimental measurements.

Chapter 5 – Simulation results validation using experimental measurements

In this chapter, the measurements presented in Chapter 3 were repeated using the design for the mechanical tension attenuation on the capacitors and layout optimization.

Fig.5.1 and Fig.5.7 present the voltage measured at the LED Driver's output. In Fig.5.1, we can observe that the 20V voltage spike was reduced to 14V, while in Fig.5.7, we can observe how the voltage pulses rise from the 5V level to the 10V level (compared with the previous case where the voltage pulse rose from 0V to 10V).

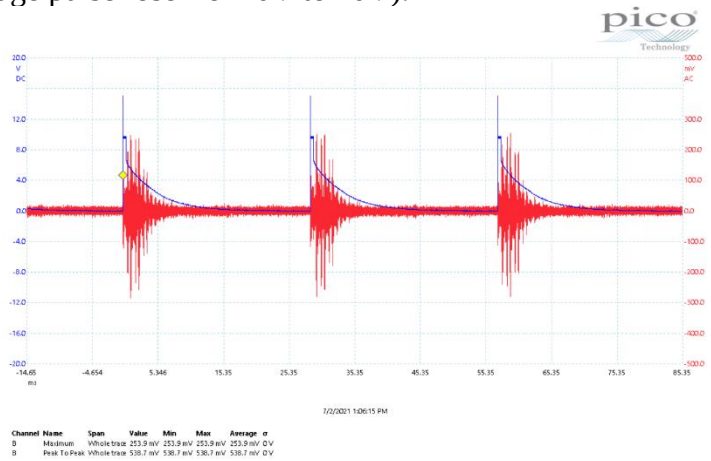


Fig.5.1. PCB vibration for the voltage spike elimination design using LED command mode 1

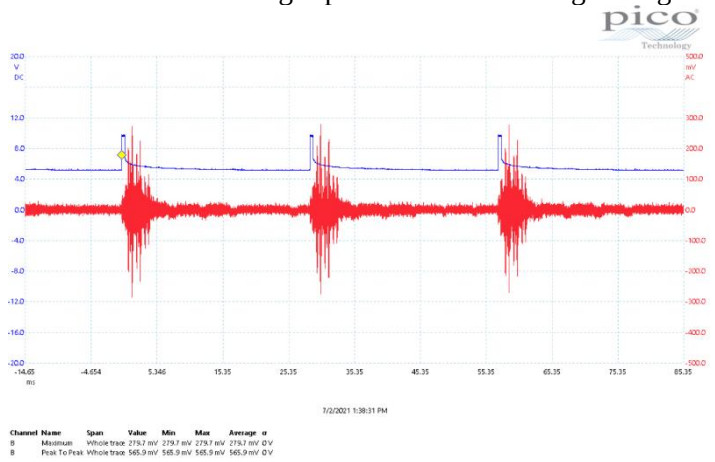


Fig.5.7. PCB vibration for the pre-charged capacitors using LED command mode 1

Using the voltage spike elimination and pre-charged capacitors designs, the acoustic noise of tens of thousands was measured in the acoustic measurement laboratory. The results are presented in Fig.5.13 – Fig.5.16, where on the horizontal axis are represented the SPL values, and on the vertical axis is represented the percentual number of devices with that specific SPL value. The results were interpolated with the Gauss's curve equation, represented in equation (5.1):

$$f(x) = A\, e^{\frac{-(x-\mu)^2}{2\sigma^2}} \tag{5.1}$$

where f(x) represents the function value for the x point on the Gauss's curve, A is a scaling constant that controls the amplitude of the curve, μ is the medium value or the Gauss's curve's center, and σ is the standard deviation which controls the curve's width.

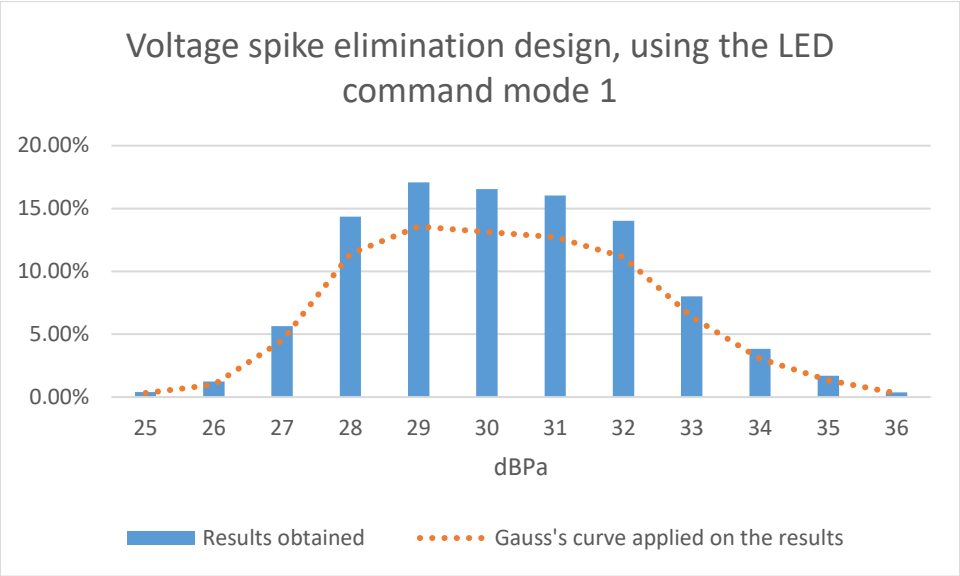


Fig.5.13. Results obtain by measuring the voltage spike elimination design, using the LED command mode 1

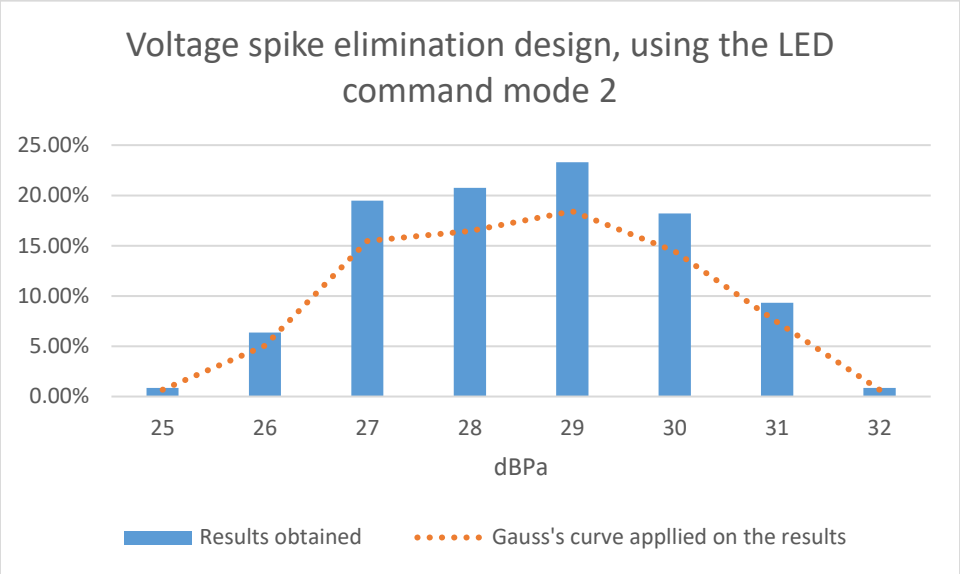


Fig.5.14. Results obtain by measuring the voltage spike elimination design, using the LED command mode 2

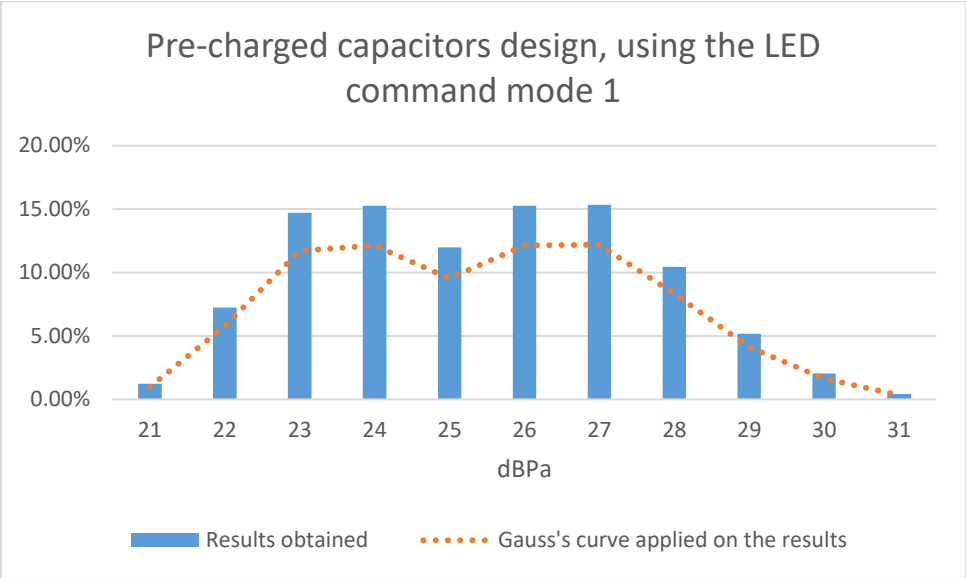


Fig.5.15. Results obtain by measuring the pre-charged capacitors design, using the LED command mode 1

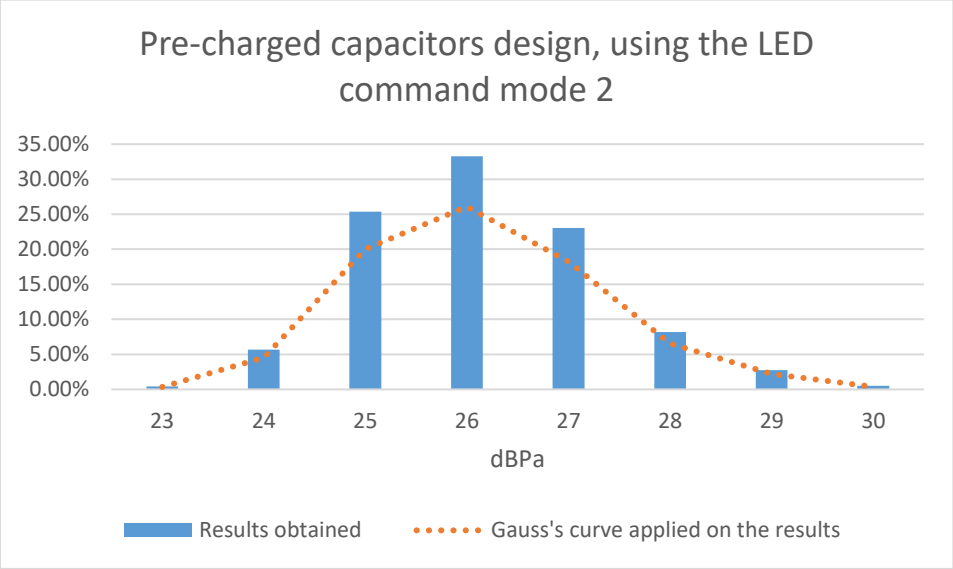


Fig.5.16. Results obtain by measuring the pre-charged capacitors design, using the LED command mode 2

As we can see, there is a large variation of the sound pressure level values from one device to another. This variation is due to the capacitor orientation on PCB. As explained in Chapter 2 – State of the art, an MLCC placed in vertical orientation generates less acoustic noise than a horizontally placed capacitor. The capacitor's orientation is also the reason why we have two Gauss's curves in Fig.5.15, where the Gauss's curve center for the capacitors placed in vertical orientation is 23dBPa, and for the horizontal orientated capacitors is 26dBPa.
This phenomenon is studied in the next chapter, where the additional solutions for the singing capacitor phenomenon are presented.
For the layout optimization, I used three different component suppliers. The results are presented in Fig.5.17 and Fig.5.18.

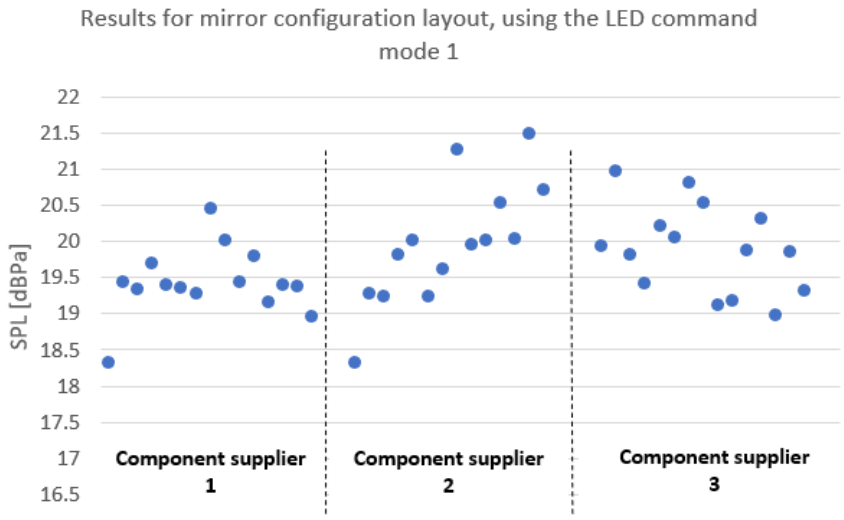


Fig.5.17. Results for mirror configuration layout, using the LED command mode 1

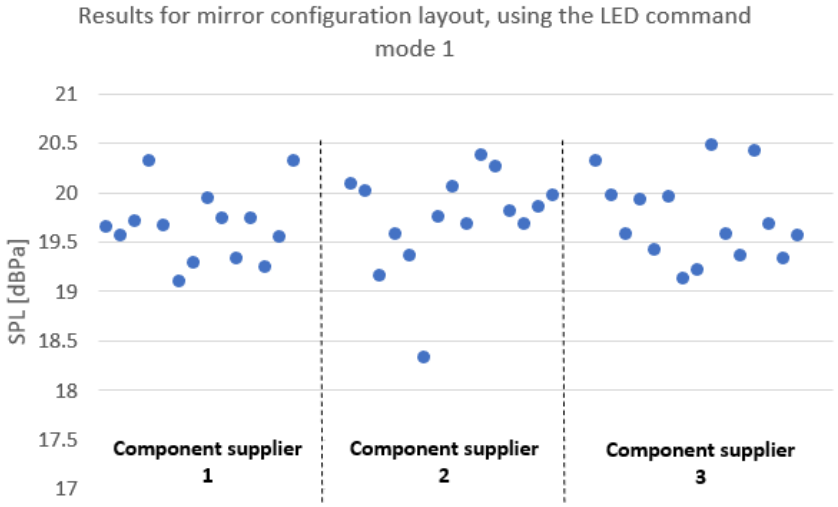


Fig.5.18. Results for mirror configuration layout, using the LED command mode 2

Similar to the harmonic simulation results, the results obtained when using the mirror layout configuration design are better compared with the mechanical tension attenuation on the design of the capacitor. For the LED command mode 1, the sound pressure level values were measured between 18.33dBPa and 21.50dBPa. Therefore, when using the mirror layout configuration, the customer's requested limit of 27dBPa is fulfilled.

Table 5.3 summarize both the simulation and measurement results obtained for the less favorable cases. In this table, I considered the results obtained only for the three-point fixation systems and the LEDs commanded using the first mode. Since the C3, C8, and C13 capacitors are not taken into consideration in the harmonic analysis, we will consider the original design simulation the correspondent for the experimental measurements using the voltage spike elimination design.

Case investigated	Maximum displacement obtained in simulation	Maximum SPL measured
Voltage spike elimination design	20.26nm	36.83dBPa
Pre-charged capacitors design	7.96nm	31.99dBPa
Mirror layout configuration design	117fm	21.50dBPa

Table 5.3. Simulation and experimental measurements result summary

Chapter 6 – Alternative solutions investigated for the singing capacitor phenomenon reduction

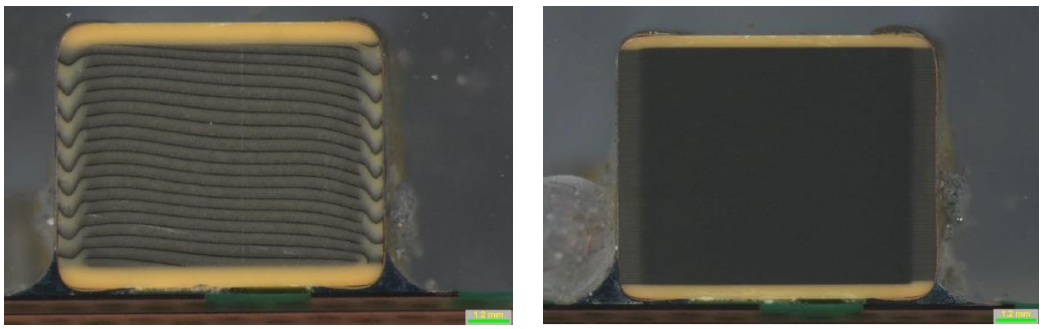
In the previous chapters, I proposed and validated two solutions for the singing capacitors phenomenon: mechanical tension attenuation on the capacitors and mirror layout configuration. In this chapter, I will propose additional alternatives for the attenuation or elimination of the acoustic noise caused by multilayer ceramic capacitors. These solutions are divided in:

- Solutions focused on the manufacturing process modification
- Solutions focused on the component modification
- Solutions to muffle de acoustic noise
- Layout optimization, this time using the parallel configuration

The first investigated solution is placing the capacitor in a vertical orientation on PCB. As mentioned in Chapter 2, in the literature, it is considered that a capacitor placed in a vertical orientation generates less acoustic noise than a capacitor placed in a horizontal orientation. We consider a capacitor placed in vertical orientation when its inner electrodes are perpendicular to PCB, and we consider it placed in horizontal orientation when its inner electrodes are parallel with the PCB.

To ease the analysis of the results, the investigation was made using only the pre-charged capacitor design, controlled with LED command mode 1. Therefore, only the C5 and C6 capacitors (which have a value of 2.2µF) generate acoustic noise.

For this investigation, I selected twenty devices with different SPL values and performed a cross-section on the C5 and C6 capacitors to determine their orientation on the PCB. Fig.6.1 presents a vertical-oriented capacitor and a horizontal-oriented capacitor.



a) b)

Fig.6.1. Capacitor cross-section: a) vertical-oriented capacitor; b) horizontal-oriented capacitors

Table 6.1 presents the orientation of the C5 and C6 capacitors, together with their corresponding SPL value. We can observe that the acoustic noise generated by the PCB is dependent on the C6 capacitor orientation, while the orientation of the C5 capacitor does not influence the SPL value. This happens due to the capacitors' position on the PCB. The C6 capacitor is placed towards the outside of the PCB, while the C5 capacitor is placed near the center of the PCB. Therefore, although both capacitors vibrate the same, the PCB vibration is mostly affected by the vibration of the capacitor placed further from the fixation points.

SPL [dBPa]	C6 capacitor orientation	C5 capacitor orientation
23.51	Verticală	Verticală
23.54	Verticală	Orizontală
23.86	Verticală	Orizontală
23.99	Verticală	Orizontală
24.03	Verticală	Orizontală
25.52	Verticală	Verticală
26.31	Verticală	Verticală
26.34	Orizontală	Orizontală
26.97	Orizontală	Orizontală
27.05	Orizontală	Orizontală
27.23	Orizontală	Verticală
27.63	Orizontală	Orizontală
28.42	Orizontală	Orizontală
28.42	Orizontală	Verticală
28.77	Orizontală	Verticală
29.37	Orizontală	Verticală
29.41	Orizontală	Orizontală
29.74	Orizontală	Verticală
31.08	Orizontală	Orizontală
31.64	Orizontală	Verticală

Tabel 6.1. Results obtained after performing the cross-section of the capacitors on twenty devices

Another possible solution mentioned in Chapter 2 is the solder paste reduction. To check this hypothesis, we reduced the stencil's thickness from 150µm to 120µm. We used this stencil to populate the components of both the voltage spike elimination design and the design of the pre-charged capacitor. As in the previous investigation, we used only the LED command mode 1, to ease the results analysis. The results are interpolated with the Gauss's curve and are presented in Fig.6.2. and Fig.6.3.

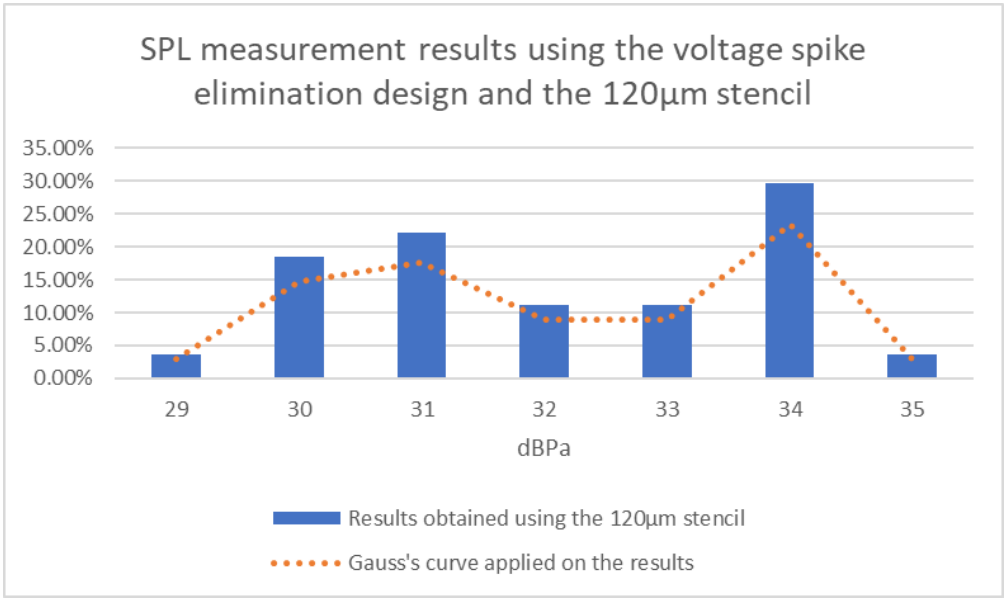


Fig.6.2. SPL measurement results using the voltage spike elimination design and the 120µm stencil

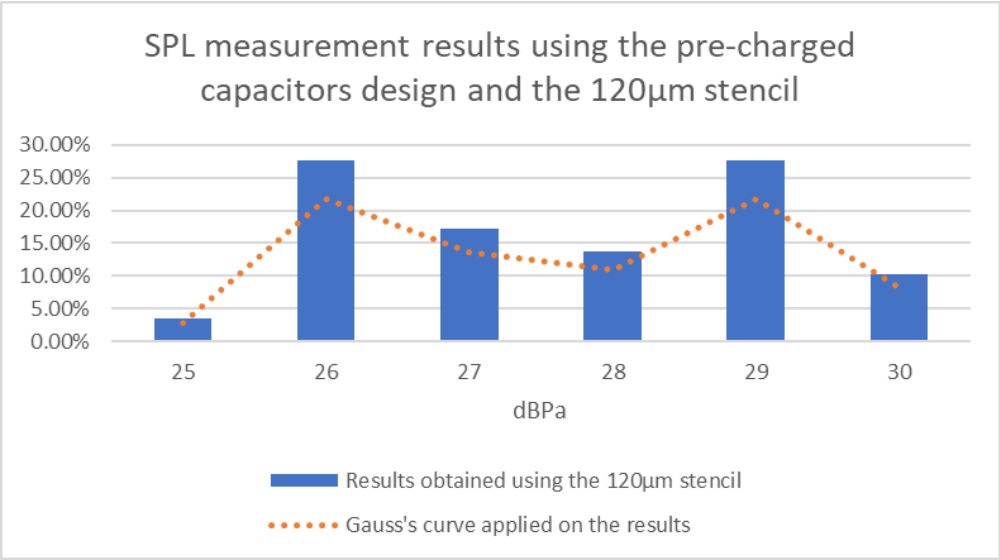


Fig.6.3. SPL measurement results using the pre-charged capacitors design and the 120µm stencil

As we can see, the results obtained using the 120µm stencil are slightly better than the results presented in Fig.5.13 and Fig.5.15, where I used the 150µm stencil. For the voltage spike elimination design, the SPL measured for the 120µm stencil was between 29dBPa and 35dBPa, while for the 150µm stencil, the results were between 25dBPa and 36dBPa. For the pre-charged capacitors, the measured SPL was between 25dBPa and 30dBPa when using the 120µm stencil and between 21dBPa and 31dBPa when using the 150µm stencil.
Although the maximum SPL value measured when using the 120µm stencil was slightly below the previous maximum value, and the sound pressure level results had a smaller variation, we must take into consideration that the number of devices tested using the 120µm stencil is significantly smaller than the number of devices tested using the 150µm stencil (30 PCBs with 120µm stencil and tens of thousands PCBs with 150µm stencil).
Therefore, the acoustic noise results are not significantly better when using a smaller quantity of solder paste. Moreover, the reduction of solder paste quantity could lead to product quality issues.
Some studies suggest that the MLCC dielectric properties are superior at high temperatures, especially at the Curie temperature of barium titanate (around 130˚C). To investigate this, I selected a few devices using the pre-charged capacitors design and I measured the SPL value in an anechoic chamber. Then, the samples were taken back to the assembly line, where I oven-cured the PCB at 130˚C for half an hour. However, the results were not improved after oven curing.
Another possible solution that could attenuate the singing capacitor phenomenon and implies modification of the manufacturing process is varnishing. For this investigation, I applied varnish on the PCB in the areas where the 2.2µF capacitors are placed, as shown in Fig.6.5.

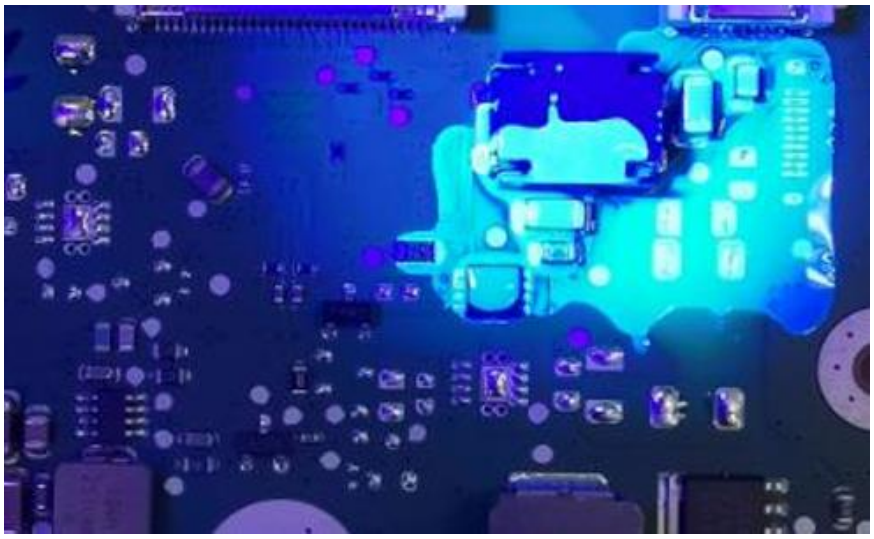


Fig.6.5. Varnish applied on the PCB, visible only when exposed to UV light

For the voltage spike elimination design, the before and after results are similar. While for the pre-charged capacitors design, the results are slightly better after varnishing.
The last investigation from the manufactory process modification category is MLCC vibration isolation using a specialized solution known as potting in the industry. Potting is the process where we apply a solid or gelatinous compound to the PCB. For our investigation, I used the DOWSIL 7091 potting material, which is a high-performance neutral polymer silicone adhesive. The potting material was applied to the problematic capacitors, as shown in Fig.6.8.

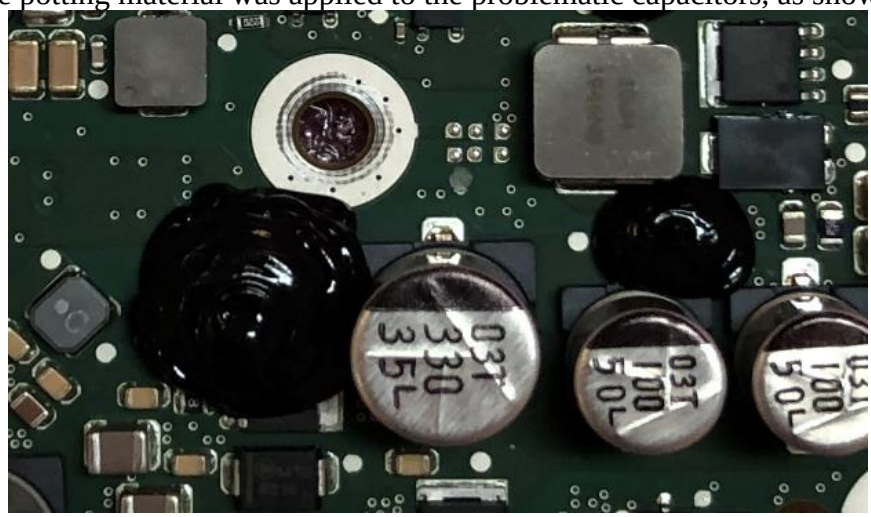


Fig.6.8. Potting applied on the PCB

The results show a 2dBPa improvement of the SPL when using potting. Therefore, the potting process could be a solution for the singing capacitor phenomenon, but it could also lead to thermal problems of the device or warranty-related issues.
For the solutions focused on the component modification category, I studied the acoustic noise behavior of the capacitors with C0G dielectric type. Up to this moment, the capacitors investigated had the dielectric type X7R, which belongs to dielectric class 2. The C0G dielectric type capacitors are class 1 capacitors, and they are known in the industry as one of the most stable capacitors available since their capacity is not significantly affected by the temperature, applied voltage, or aging.
I replaced the 2.2µF capacitors with a series of C0G capacitors placed in parallel (with equivalent capacitance) to observe the acoustic noise behavior. Similar to previous

measurements, the device was turned on for 10s and then turned off for another 10s to observe the anechoic chamber reference level. Fig.6.13 presents the X7R dielectric type capacitors' SPL value, while Fig.6.14 presents the C0G dielectric type capacitors' SPL value.

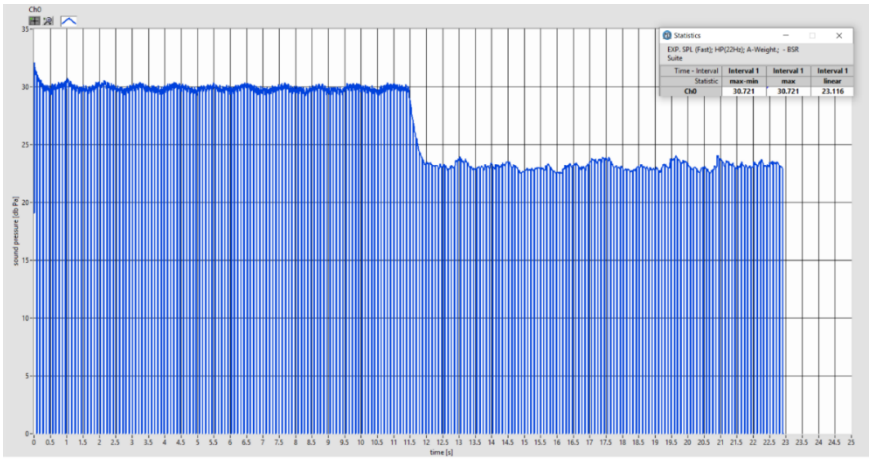


Fig.6.13. Measurement results for the X7R dielectric-type capacitors

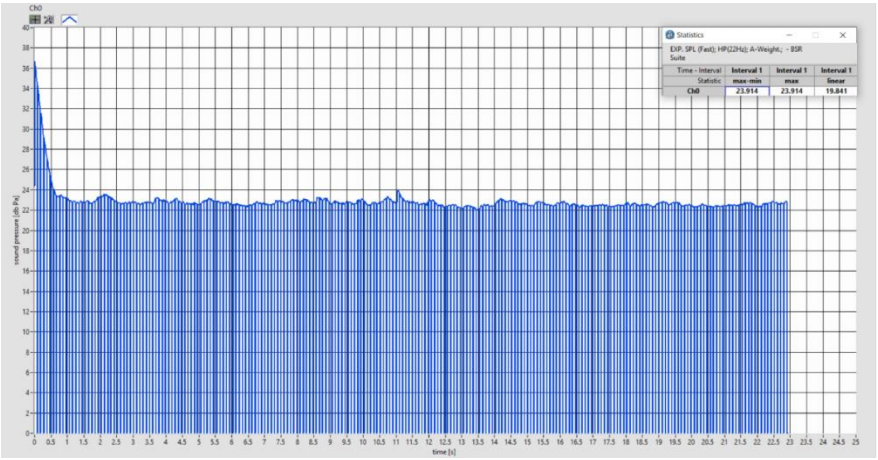


Fig.6.14. Measurment results for the C0G dielectic-type capacitors

As we can observe when we used the X7R dielectric-type capacitors, the measured SPL was 30dBPa. When we replaced these capacitors with C0G dielectric-type capacitors, the SPL value was 24dBPa (identical to the anechoic chamber's reference level).
The acoustic noise improvement when using the C0G dielectric-type capacitors is incontestable. However, the required space on the PCB to use this type of component to replace the 2.2µF capacitors is significantly increasing. Therefore, this solution is not feasible for systems with restrictive size requirements.
In some cases, because of either the design development phase or price concern, the best solution is to prevent the acoustic noise to reach the user's ear, by muffling. There are two sound transmission paths: through structure and air. To eliminate the structure-transmitted acoustic noise, one solution is anti-vibration grommets. These grommets isolate the system vibration from the rest of the car. They are made of EPDM (Ethylene Propylene Diene Monomer) rubber and are mounted on the fixation holes. To eliminate the air-transmitted acoustic noise, foam can be used. In our case, the only path the sound can be transmitted through the air is the space between the connector and the product case. To muffle the sound, we used a special fireproof sponge made of semi-closed cell EPDM.
In Chapter 4, I propose the mirror layout configuration optimization solution, and I demonstrated its efficiency in Chapter 5. However, in Table 2.1, it is highlighted that when

using regular-type capacitors, besides mirror layout configuration, parallel layout optimization is also efficient.
To investigate this solution, similar to the mirror layout configuration solution, I replaced every 2.2µF capacitor (with 1206 package footprint) with a pair of 1µF capacitors (with 0805). I started again from the design of the pre-charged capacitor, but in this case, the capacitors were placed in parallel, on the same side of the PCB. As shown before, we used three different component suppliers. The results are presented in Fig.6.18.

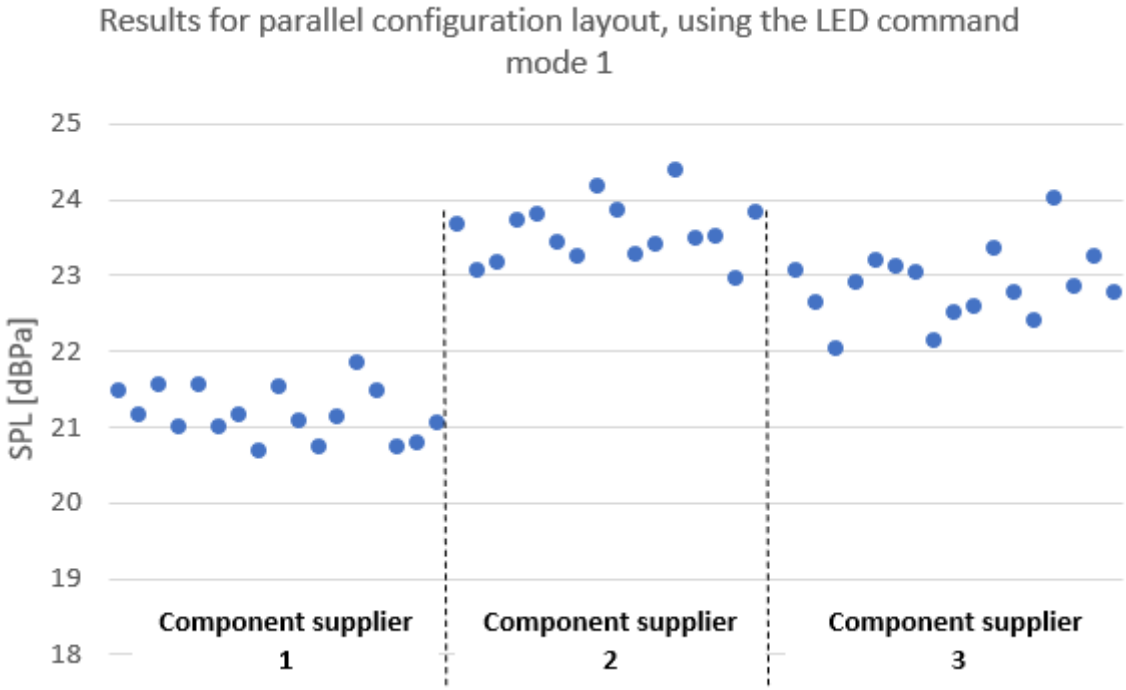


Fig.6.18. Results obtained using the parallel layout configuration and the LED command mode 1

The first observation is that the obtained results are better, compared with the results presented in Fig.5.15, where the maximum SPL value is 31dBPa. The second observation is that the results are dependent on the component supplier when using the parallel layout configuration. As presented in Fig.6.18, the capacitors from the first component supplier are more silent, while the acoustic noise generated by the capacitors from the second supplier is higher.
Table 6.2 presents a summary of the proposed solutions in this paper.

Category	Proposed solution	Efficiency	Observations	Additional cost
Design modification	Mechanical tension attenuation on the capacitors	++	The solution is dependent on the product design	Additional cost to modify the design
	Layout optimization	+++	The solution is dependent on the product design and the type of capacitor used	Additional cost to modify the design
Manufacturing process modification	Solder paste quantity reduction	+	Could lead to quality issues	The cost is not affected (it is slightly improved due to the reduced solder paste quantity)
	Oven curing	-	-	Additional cost to add the oven curing step in the manufacturing process
	Varnishing	+	-	Additional cost to add the varnishing step in the manufacturing process
	Potting	++	Could lead to thermal issues or warranty-related issues	Additional cost to add the potting step in the manufacturing process
	Vertical orientation placement of the capacitors	+++	The capacitors can be preselected by the supplier	Additional cost due to the preselected components
Component modification	Commercially available capacitors	++++	This solution was not investigated experimentally, but their results are presented in Chapter 2	Alternative component cost
	C0G dielectric-type capacitors	++++	Besides the expensive price, the C0G dielectric-type capacitors require more space on the PCB than the class 2 capacitors	C0G dielectric-type capacitors
Muffling solutions	Anti-vibration grommets	++	Could require packaging modifications or assembly jig modifications	Anti-vibration grommets cost and the assembly jig modification cost
	EPDM foam	++	Can be hard to implement in an automatic assembly process	Additional cost in the manufacturing process to add the foam

Tabel 6.2. Investigated solution summary

Chapter 7 – Conclusions and original contributions

This paper studies the acoustic noise caused by multilayer ceramic capacitors in electronic devices. To obtain advantages such as small dimensions, small price, large capacitance domain, and favorable electric characteristics, most of the MLCCs have dielectric material made of barium titanate. The main electromechanical properties of barium titanate are piezoelectricity and electrostriction. Due to these properties, when we apply an alternative voltage on the capacitor, the dielectric material expands on the electric field direction, causing the PCB deformation. When this deformation reaches the resonance frequency in the audible range of 20Hz-20kHz, the phenomenon known as singing capacitors appears.

This paper is an applicative research, where I study the singing capacitor phenomenon presence in a module (LED Driver) developed by Continental Automotive™. The module generates 4A pulses, with a 470µs width and 35Hz frequency, applied on six 2.2µF multilayer ceramic capacitors.

Initially, we used two methods to measure the singing capacitor phenomenon: vibration measurement using a piezoelectric accelerometer and acoustic measurement using a microphone placed in an anechoic chamber. The acoustic measurement was more accurate; therefore, I continued the investigations using identical conditions for acoustic measurement.

In the simulation chapter, the first step was to determine the difference between the three-point and four-point fixation, from the mechanical vibration point of view. Initially, I released a modal analysis of the two fixation modes, but the results did not present a significant difference in the modal shapes. Therefore, I released a harmonic analysis, where taking into consideration the populated components and PCB-related information, I applied a 2Pa force on each problematic capacitor. It was demonstrated that in the four-point fixation, the maximum PCB displacement was smaller than the three-point fixation displacement.

Afterward, I proposed two methods to attenuate the singing capacitor phenomenon. The first proposal focused on the mechanical tension attenuation on the capacitor, while the second proposal focused on the layout optimization by placing the capacitors in a mirror configuration. The harmonic analysis results presented an improvement in the system vibration: the design with the pre-charged capacitor had a smaller maximum displacement than the original design, and the layout optimization design had a smaller maximum displacement than the previous proposal. These results are summarized in Table 4.2, and they were experimentally validated in Chapter 5.

In Chapter 6, I proposed additional alternatives to reduce the singing capacitors phenomenon and analyzed them from the efficiency point of view. These proposals are divided into four categories: solutions focused on the manufacturing process modification, solutions focused on the component modifications, solutions to muffle the sound, and layout optimization. For the solutions focused on the manufacturing process modification category, I proposed placing the capacitor in a vertical orientation, solder paste reduction, oven curing, varnishing, and potting. Since the commercially available solutions are already investigated in Chapter 2, for the solutions focused on the component modifications, I studied the acoustic effect of using the class 1 capacitors (C0G dielectric-type capacitors). For sound muffling, I propose the anti-vibration grommets and the special fireproof sponge made of semi-closed cell EPDM. The chapter ends with a layout optimization proposal by placing the capacitors in a parallel configuration. The investigation results are presented in Table 6.2.

The **original contributions** in this paper are:

Chapter 2 – State of the art

- Structuring and comparative information analysis from current specialized literature;
- Explanation of the "singing capacitors" phenomenon using visual representations (Fig.2.1 and Fig.2.2);
- Synthesizing the solutions to minimize the analyzed phenomenon, presented in Fig. 2.3;
- Comparative representation of commercially available solutions (Fig.2.4, Fig.2.5, Fig.2.7 - Fig.2.10);
- Description of the optimal geometric configurations for the placement of multilayer ceramic capacitors (Fig.2.11 – Fig.2.13);
- Description of an alternative method of placing the soldering paste (Fig. 2.15);
- Summary of the efficiency of the layout configurations in Table 2.1;
- Comparative analysis of solutions to minimize the phenomenon analyzed in Table 2.2.

Chapter 3 – Detailed analysis of the issue

- Highlighting the dependence of vibration on the electrical signal in Fig.3.4 and Fig.3.5;
- Differential analysis of the two command modes in Table 3.2, highlighting the better results associated with command mode 1.

Chapter 4 – Simulation

- Proposal of a method to mitigate the mechanical stress applied to capacitors by eliminating voltage spikes in Fig. 4.17;
- Proposal of a method to mitigate the mechanical tension applied to capacitors by pre-charging them in Fig.4.18;
- Layout optimization proposal by placing the components in a mirror configuration in Fig.4.25;
- Analysis and synthesis of the results obtained through simulation.

Chapter 5 – Simulation results validation using experimental measurements

- Experimental validation of the proposed method of mitigating the mechanical tension applied to capacitors by eliminating voltage spikes (Fig.5.1 – Fig.5.6, respectively Fig.5.13 – Fig.5.14);
- Experimental validation of the proposed method of mitigating the mechanical tension applied to capacitors by pre-charging them (Fig.5.7 – Fig.5.12, respectively Fig.5.15 – Fig.5.16);
- Summarization of the comparative results obtained following the measurement of the original design, respectively of the two methods of mitigating the mechanical tension applied to the capacitors, in Table 5.1 and Table 5.2;

Chapter 6 – Alternative solutions investigated for the singing capacitor phenomenon reduction

- Analysis of the effect of positioning the capacitor in a vertical or horizontal position on the acoustic noise generated by it and the manufacturing process;
- Analysis of the effect of reducing the amount of soldering paste on the PCB on the "singing capacitors" phenomenon and the quality of the product;
- The interpretation of the results regarding the oven curing of the PCB led to the conclusion that this is not a solution for reducing the acoustic noise generated by

multilayer ceramic capacitors;

- Investigation of the results obtained after PCB varnishing;
- Analysis of the process of protecting capacitors through a specialized solution (potting) on acoustic noise;
- Proposal to use the class 1 capacitors and presentation of the space restrictions;
- Proposal to use the anti-vibration grommets and the EPDM foam as methods of muffling the sound transmitted through the structure, respectively air;
- Layout optimization proposal by placing components in a parallel configuration;
- Synthesis of the results obtained together with observations regarding their efficiency and costs involved, in Table 6.2.

List of published scientific papers, related to the singing capacitor phenomenon:

1. Covaci, C., & Gontean, A. (2020). Piezoelectric Energy Harvesting Solutions: A Review. Sensors, 20(12), 3512. doi:10.3390/s20123512 – Cited 166 times, it was in 1% top of most cited papers in the chemistry academic domain, and it received the „2022 Best Paper Award" from MDPI
2. Covaci, C., & Gontean, A. (2022). "Singing" multilayer ceramic capacitors and mitigation methods — a review. Sensors, 22(10), 3869. doi:10.3390/s22103869 – Cited 2 times
3. Covaci, C., Burza, F., & Krausz, T. (2022). MLCC acoustic noise mitigation via appropriate design. 2022 IEEE 9th Electronics System-Integration Technology Conference (ESTC). doi:10.1109/estc55720.2022.9939506
4. Covaci, C., Burza, F., & Gontean, A. (2022). Solutions for acoustic noise caused by multilayer ceramic capacitors. 2022 IEEE 28th International Symposium for Design and Technology in Electronic Packaging (SIITME). doi:10.1109/siitme56728.2022.9988700

List of additional published scientific papers during the thesis elaboration:

1. Covaci, C., & Gontean, A. (2018). Spice model of a piezoelectric transducer. 2018 IEEE 24th International Symposium for Design and Technology in Electronic Packaging (SIITME). https://doi.org/10.1109/siitme.2018.8599212
2. Covaci, C., & Gontean, A. (2019). Energy harvesting with piezoelectric materials for IOT – Review. ITM Web of Conferences, 29, 03010. https://doi.org/10.1051/itmconf/20192903010 - neindexată în WoS
3. Covaci, C., Porobic, I., & Gontean, A. (2019). Setup for Piezoelectric Energy Harvesting System. 2019 IEEE 25th International Symposium for Design and Technology in Electronic Packaging (SIITME). https://doi.org/10.1109/siitme47687.2019.8990858
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5. Covaci, C., & Gontean, A. (2021). Piezoelectric energy harvesting using SSHI technique. 2021 IEEE 27th International Symposium for Design and Technology in Electronic Packaging (SIITME). https://doi.org/10.1109/siitme53254.2021.9663643

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3. Lu, T., Ding, M., & Wu, K. (2019). Simulation and characterization of singing capacitors in consumer electronics. 2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI). doi:10.1109/isemc.2019.8825286
4. Yu, D., Dai, K., Zhang, J., Yang, B., Zhang, H., & Ma, S. (2020). Failure mechanism of multilayer ceramic capacitors under transient high impact. Applied Sciences, 10(23), 8435. doi:10.3390/app10238435
5. Sun, Y., Zhang, J., Yang, Z., Hwang, C., & Wu, S. (2019). Measurement investigation on acoustic noise caused by “singing” capacitors on mobile devices. 2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI). doi:10.1109/isemc.2019.8825220
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