Universitatea Politehnica Timișoara

Facultatea de electronică, telecomunicații și tehnologii informaționale

HABILITATION THESIS
TEZĂ DE ABILITARE

DC-DC Converters – Architectures, Control and Applications
Convertoare CC-CC– Architecturi, Comandă și Aplicații

Domeniul de doctorat:
Inginerie electronică telecomunicații și tehnologii informaționale

Dr. eng. Ioana-Monica POP-CĂLIMANU

2025

Contents

Rezumat

Prezenta teză de abilitare, intitulată "Convertoare DC-DC - Arhitecturi, Comandă și Aplicații", oferă o analiză cuprinzătoare a contribuțiilor originale aduse în domeniul electronicii de putere, în special în domeniul convertoarelor DC-DC.

Începând cu un rezumat atât în limba română cât și în limba engleză, teza continuă cu o sinteză a cercetărilor efectuate în cadrul studiilor de doctorat. Aceasta prezintă principiile fundamentale ale convertoarelor DC-DC și clasificarea lor, acoperind arhitecturi clasice, bidirecționale și topologii hibride. Se oferă o analiză detaliată a tipurilor de celulele de comutație, subliniind rolul configurațiilor de comutație *L* și *C* în obținerea unei conversii de energie cu randament ridicat. Este realizată o analiză comparativă a topologiilor de convertoare DC-DC existente, identificându-se limitările și domeniile în care pot fi aduse îmbunătățiri în ceea ce privește randamentul, raportul static de conversie, solicitările și numărul de componente. Capitolul prezintă, de asemenea, motivația pentru dezvoltarea de noi familii de convertoare hibride, subliniind avantajele lor potențiale comparativ cu modelele convenționale. În plus, se introduce o metodă sistematică de sinteză a noilor convertoare hibride multifază.

Partea cu greutate a tezei de abilitare este prezentată în capitolul 2. Acest capitol este o trecere în revistă a realizărilor în domeniul științific, profesional și academic după susținerea tezei de doctorat. Lucrarea se concentrează pe cercetarea științifică realizată după doctorat, detaliind contribuțiile propuse în ceea ce privește topologiile convertoarelor DC-DC, metodele de control și aplicațiile acestora.

Tematica cercetării științifice a fost împărțită în patru subiecte de bază:

1. Dezvoltarea de noi familii de convertoare DC-DC, propunând topologii hibride inovatoare care cresc randamentul și performanțele. Sunt introduse mai multe structuri noi de convertoare, printre care convertoarele Buck-*L*, Boost-*L*, Buck-Boost-*L* și Ćuk-*L*, fiecare dintre acestea fiind conceput pentru a îmbunătăți conversia puterii în diferite aplicații.

Unele dintre aceste convertoare utilizează bobine cuplate, comutație întrețesută și tehnici avansate de comandă pentru a reduce pierderile și a îmbunătăți stabilizarea tensiunii. Strategia utilizată pentru generarea acestor noi topologii de convertoare este fundamentată prin intermediul unei modelări matematice riguroase, simulări de circuit și validări experimentale.

Analizele comparative cu topologiile tradiționale confirmă superioritatea noilor convertoare, constând în câștiguri de tensiune mai mari sau mai mici, solicitări de tensiuni si curenti mai mici și randament mai mare. Simulările au validat aspectele teoretice dezvoltate. În plus, toate prototipurile experimentale ale convertoarelor propuse au confirmat fezabilitatea acestora în practică, ceea ce corespunde îndeaproape prognozelor analitice și simulărilor.

2. Metodele de comandă pentru convertoarele DC-DC sunt orientate către stabilitate, fenomene de bifurcație și proiectarea controlerului. Se efectuează o analiză a stabilității unui convertor boost cu două faze, evidențiind parametrii cheie care afectează performanțele sistemului și răspunsul tranzitoriu. Studiile de bifurcație ale funcționării în modul de conducție discontinuu (DCM) evidențiază comportamentele neliniare și potențialele probleme de instabilitate în condiții de parametrii variabili. În plus, este prezentat un proces sistematic de proiectare pentru un convertor buck-boost ideal de ordinul patru, optimizând strategiile de comandă pentru îmbunătățirea stabilizării tensiunii și creșterii randamentului. Este dezvoltat un controler pentru un

convertor cu pierderi pătratic de tip buck, care asigură robustețea împotriva perturbațiilor sistemului.

3. O aplicație a convertoarelor propuse este domeniul energiilor regenerabile, în special al sistemelor fotovoltaice (PV) și al pilelor de combustie. Utilizarea convertoarelor DC-DC în sistemele fotovoltaice se concentrează pe îmbunătățirea randamentului și pe valorificarea energetică sporită. A fost introdus un convertor hibrid de tip boost, conceput special pentru a optimiza conversia ridicătoare a tensiunii pentru aplicațiile fotovoltaice. În plus, este propus un convertor DC-DC SEPIC cu bobine cuplate pentru a obține un raport static de conversie ridicat, reducând în același timp solicitarea în curent și tensiune a componentelor și pierderile de putere. Simulările și experimentele efectuate au validat performanța superioară a acestor convertoare în ceea ce privește câștigul în tensiune și răspunsul dinamic îmbunătățit. Capitolul evidențiază rolul important al electronicii de putere avansate în maximizarea randamentului sistemelor de energie regenerabilă.

4. Optimizarea grupului propulsor al vehiculelor cu baterii și pile de combustie hibride. Este introdusă o nouă strategie de comandă pentru distribuția energiei în vehiculele hibride cu baterii și pile de combustie, asigurând gestionarea eficientă a energiei și prelungirea duratei de viață a bateriei. Se propune un convertor DC-DC multifază pentru a îmbunătăți performanța grupului propulsor, reducând pulsațiile curenților de intrare și de ieșire și îmbunătățind randamentul general. În plus, este dezvoltat un banc de testare dedicat pentru a optimiza configurațiile grupului propulsor, validând conceptele de convertoare propuse prin analize experimentale. Studiul explorează și convertoarele DC-DC bidirecționale pentru frânarea regenerativă, permițând recuperarea energiei și îmbunătățirea randamentului pilelor de combustie.

Teza de abilitare evidențiază contribuțiile academice și profesionale ale autorului, punându-se accentul pe predare, diseminarea cercetării și colaborare cu industria și mediul academic. Sunt detaliate meritele autorului în publicarea în reviste cu factor impact ridicat: 9 articole WoS (anterior ISI) și 44 de articole publicate în volumele conferințelor (32 de articole WoS și 12 BDI), demonstrând recunoașterea internațională și națională a activității sale în domeniul electronicii de putere. Candidata a condus 2 granturi naționale, câștigate prin competiție și a participat în calitate de membru la alte 3. Capitolul subliniază contribuțiile în îndrumarea și coordonarea a 85 de studenți la finalizarea lucrărilor de licență și disertație (63 de licență și 22 de disertație) și peste 20 de masteranzi îndrumați în activitatea de cercetare, promovând astfel următoarea generație de tineri cercetători în electronică aplicată. Au fost abordate proiecte de cercetare în colaborare, demonstrând astfel integrarea competențelor multidisciplinare în electronica de putere avansată. În plus, este subliniat rolul autorului în dezvoltarea curriculumului și îmbunătățirea programelor academice de studii, contribuind la creșterea calității educației inginerești. Acest capitol subliniază aportul autorului atât în ceea ce privește inovarea în domeniul academic, cât și în cel științific.

Ultima parte este destinată unei prognoze a viitoarelor activități academice, profesionale și de cercetare, lucrarea încheindu-se cu o listă consistentă de referințe bibliografice.

Abstract

The present habilitation thesis, entitled "DC-DC Converters – Architectures, Control and Applications," provides a comprehensive analysis of the novel contributions brought to the field of power electronics, specifically in the domain of DC-DC converters.

Starting with an abstract both in Romanian and English, the thesis continues with the summary of research conducted in the PHD studies. It introduces the fundamental principles of DC-DC converters and their classification, covering classical, bidirectional and hybrid topologies architectures. It provides an in-depth review of switching cell structures, emphasizing the role of *L* and *C*-switching configurations in achieving high-efficiency energy conversion. A comparative analysis of existing DC-DC converter topologies is conducted, identifying the limitations and the areas for improvement in terms of efficiency, static conversion ratio and component count. The chapter also presents the motivation for developing novel hybrid converter families, highlighting their potential advantages compared to conventional designs. Additionally, a systematic method for synthesizing new multiphase hybrid converters is introduced, paving the way for these innovative topologies proposed in subsequent chapters.

The main part of the habilitation thesis is presented in Chapter 2. This is an overview of the achievements in scientific, professional and academic field after the PhD thesis was defended in 29.06.2015, at the Faculty of Electronics, Telecommunications and Information Technologies from Politehnica University of Timisoara. It focuses on the scientific research conducted post-PhD, detailing the proposed novelty in DC-DC converter topologies, control methods, and applications,

The focus on scientific research was divided into four key research topics:

1. The development of new families of DC-DC converters, proposing innovative hybrid topologies that improve efficiency and performance, is the first one. Several novel converter structures are introduced, including the Buck-*L*, Boost-*L*, Buck-Boost-*L* and Ćuk-*L* converters, among others, each designed to enhance power conversion for various applications.

Some of these converters employ coupled inductors, interleaved switching, and advanced control techniques to reduce the losses and improve voltage regulation. The strategy used for generating this new converter topologies is substantiated through rigorous mathematical modelling, circuit simulations, and experimental validations.

Comparative analyses with traditional topologies confirm the superiority of these new converters, consisting of higher or lower voltage gain, improved lower voltage or current stresses and higher efficiency. The simulations validated the theoretical considerations developed. Furthermore, the experimental prototypes of the proposed converters all confirmed their practical feasibility, closely matching with the analytical and simulations predictions.

2. The control methods for DC-DC converters are focusing on stability, bifurcation phenomena, and advanced controller design. A stability analysis of a two-phase boost converter is conducted, revealing the key parameters affecting system performance and transient response. Bifurcation studies of discontinuous conduction mode (DCM) operation, highlight nonlinear behaviours and potential instability issues under varying load conditions. Additionally, a

systematic design process for an ideal fourth-order buck-boost converter is presented, optimizing control strategies for improved voltage regulation and efficiency. A refined controller for a fourth-order lossy quadratic buck converter is developed, ensuring robustness against system disturbances. These control strategies provide improved transient response, reduced output voltage ripple, and enhanced system stability, making the proposed converters more reliable for industrial and commercial applications.

3. A major application of the converters proposed is the field of renewable energies, particularly the photovoltaic (PV) and fuel cell systems. The usage of DC-DC converters in PV systems focuses on efficiency improvements and enhanced energy harvesting. A new hybrid inductor-based boost converter has been introduced, specifically designed to optimize step-up voltage conversion for PV applications. Additionally, a SEPIC-based DC-DC converter with coupled inductors is proposed to achieve high step-up capability, while reducing component stress and power losses. These innovative architectures enable better integration of solar energy into modern power grids, increasing the overall system efficiency. The simulations and the experiments conducted validated the superior performance of these converters in terms of voltage gain, reduced ripple, and improved dynamic response. The chapter highlights the critical role of advanced power electronics in maximizing the effectiveness of renewable energy systems.

4. Furthermore, the thesis extends its contributions to the powertrain optimization of battery-fuel cell hybrid vehicles. A novel control strategy for power distribution in battery-fuel cell hybrid vehicles is introduced, ensuring efficient energy management and prolonged battery life. A multiphase DC-DC converter is proposed to enhance powertrain performance, reducing input and output current ripple and improving overall efficiency. Additionally, a dedicated test bench is developed to optimize powertrain configurations, validating the proposed converter designs through experimental analysis. The study also explores bidirectional DC-DC converters for regenerative braking, enabling energy recovery and improved fuel cell efficiency.

The habilitation thesis also highlights the academic and professional contributions of the author, focusing on research dissemination, teaching, and collaboration with industry and academia. It details the author's merits in publishing in high-impact journal publications: 9 WoS (formerly ISI) papers and 44 conference proceedings papers (32 WoS and 12 BDI papers) showcasing the global recognition of her work in power electronics. The candidate conducted 2 national grants and participated as a member in other 3. The chapter also emphasizes the contributions in mentoring and supervising students, 85 students in graduation bachelor and dissertation thesis (63 bachelor and 22 dissertation), and more than 20 master students guided in the research activity, thus fostering the next generation of researchers in applied electronics. Collaborative research projects are discussed, demonstrating the integration of multidisciplinary expertise in advanced power electronics. Additionally, the author's role in curriculum development and academic programs improvement is outlined, contributing to enhanced engineering education. Overall, this chapter underscores the author's influence in both scientific innovation and academic leadership.

The last part is devoted to the future academic, professional and research activities, while the work ends with a comprehensive references list.

1. Summary of research conducted in the PhD studies

The global efforts to reduce carbon emissions and the transition to sustainable energy intensify around the word. Usage of renewable energies is crucial in this context because it produces little greenhouse gases during operation. This significantly reduces the carbon footprint compared to fossil fuels, which are major contributors to global warming and climate change. As the demand for renewable energies technologies is continuously growing, the importance of DC-DC converters in ensuring efficient power flow and control is becoming increasingly evident. DC-DC converters are essential components in renewable energy systems, playing a critical role in the efficient conversion and management of electrical power, particularly in photovoltaic (PV) applications. These applications require DC-DC converters for step-up or step-down the input voltage with high efficiency. Classical DC-DC converters struggle to achieve very high conversion ratios, and using transformers for this purpose often reduces efficiency. In this context, in the PhD study [1], 11 new topologies of multiphase hybrid DC-DC converter were proposed by the author.

The PhD dissertation aimed to achieve the following objectives:

- To conduct a comprehensive review of the main DC-DC converters used in renewable energy systems as documented in the literature.
- analyze and compare the structures of the switching cells.
- To evaluate and compare different topologies of hybrid converters.
- To present a synthesizing method for generating new multiphase hybrid converters.
- To propose a new class of multiphase DC-DC converter topologies based on hybrid structures.
- To perform both analytical and digital simulation studies of the proposed converters.
- To construct and test laboratory prototypes to practically validate the theoretical results and simulations.

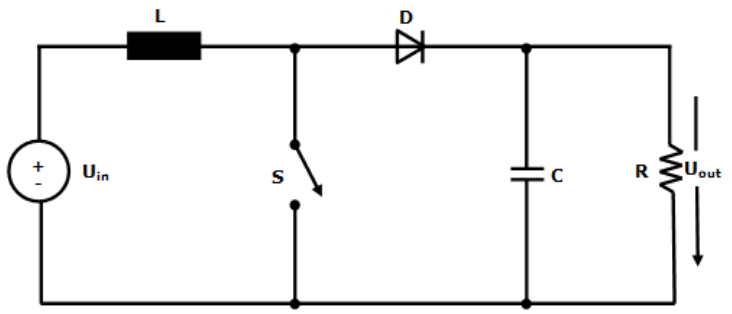
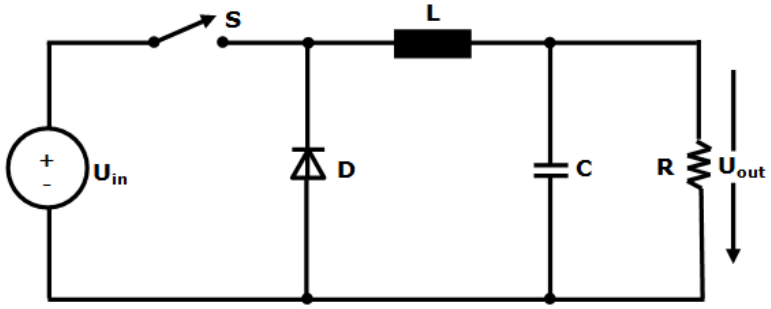
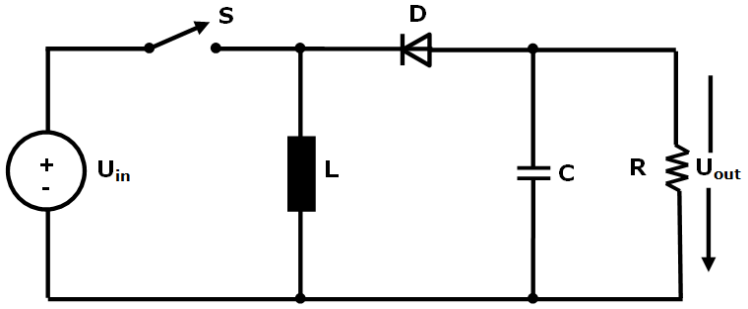
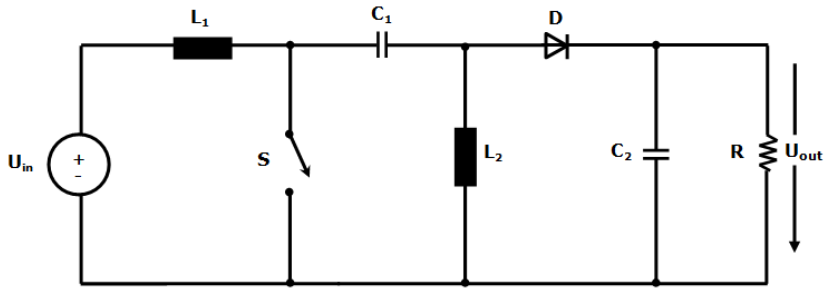
Because chapters and paragraphs of the thesis will be further referenced, it was decided to maintain the notation used in the PhD thesis. The same will apply to the papers that will be referenced in this work.

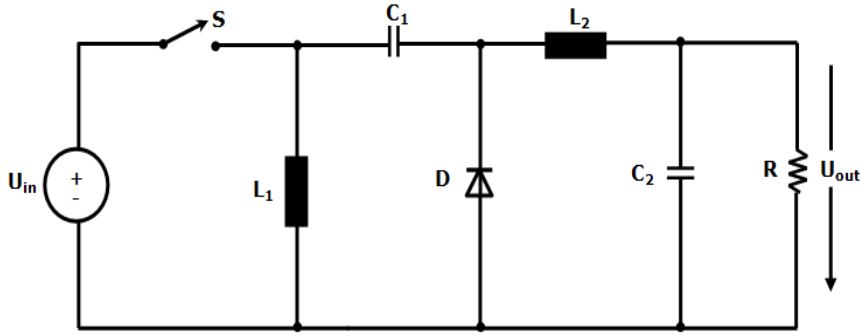
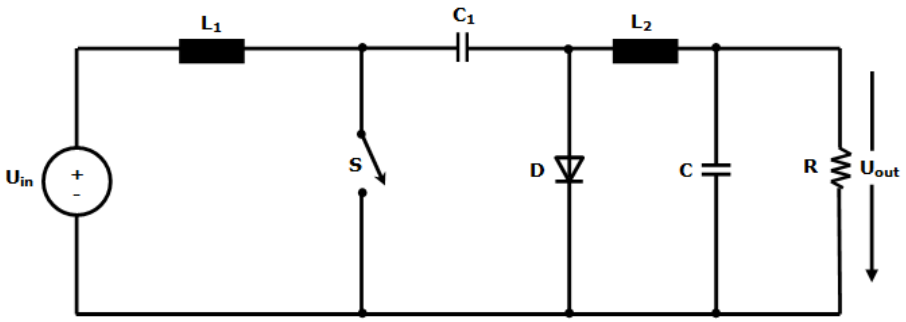
The PhD thesis was structured into five chapters, organized as follows.

Chapter 1 serves as a general introduction of the DC-DC converters encountered in the literature and used in renewable energy, emphasizing the key components of the converter. The DC-DC converters were classified into three categories: classical converters, bidirectional converters, and associations of converters. Each converter was accompanied by a circuit diagram, a brief circuit description, the static conversion ratio, the main waveforms, along with a discussion of their advantages and disadvantages. Special focus was on the classical and multiphase converters, which were the primary concerned of the thesis. The chapter ends with the presentation of a low-cost system for testing and monitoring the performance of PV modules in outdoor conditions. From this chapter, the converters that will be used in the subsequent research together with the static conversion ratio were selected and presented in Table 1.1. These converters will serve as the foundational models for development of new converter topologies in future studies. The well-known general formula for static conversion ratio is:

$$M = \frac{U_{out}}{U_{in}} \quad (1.1)$$

Table 1.1 Main converter topologies [2] - [3].

Converter name	Converter diagram	Static conversion ratio
Boost converter		$M = \frac{1}{1-d}$
Buck converter		$M = d$
Buck-Boost converter		$M = -\frac{d}{1-d}$
Sepic converter		$M = \frac{d}{1-d}$

Zeta converter		$M = \frac{d}{1-d}$
Ćuk converter		$M = -\frac{d}{1-d}$

In the second chapter the *L* and *C*-switching structures proposed by Boris Axelrod, Yefim Berkovich, and Adrian Ioinovici [4] - [5], [6], were presented and then they are integrated into classical and bidirectional converters to create new hybrid converter architectures. These hybrid structures, known as *C*-switching (using capacitors and diodes) and *L*-switching (using inductors and diodes), are presented in Table 1.2, with the possible hybrid converter topologies and their conversion ratios detailed in Table 1.3, finally offering significantly higher step-up or step-down conversion ratios compared to traditional converters.

Table 1.2 *C* and *L*-switching structures [1] - [5], [6], [7].

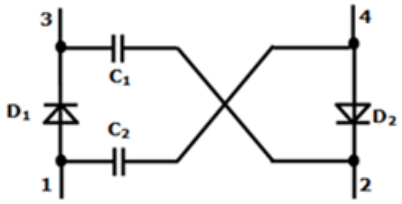
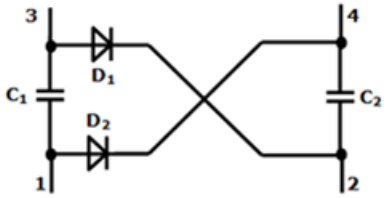
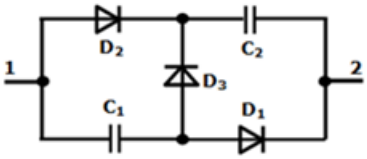
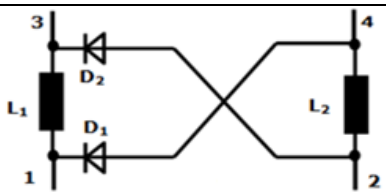
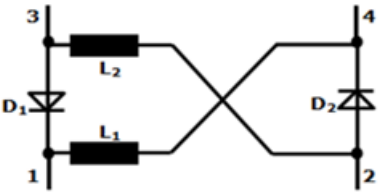
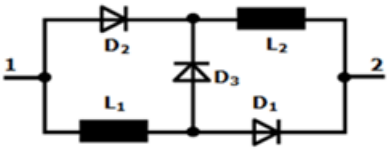
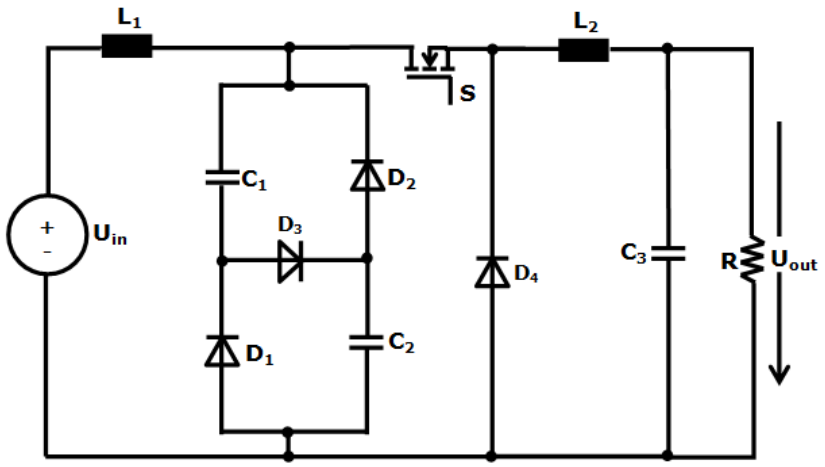
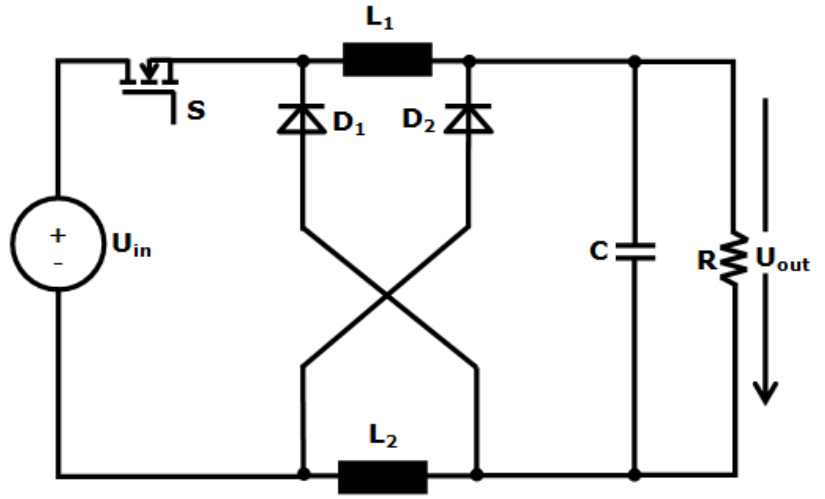
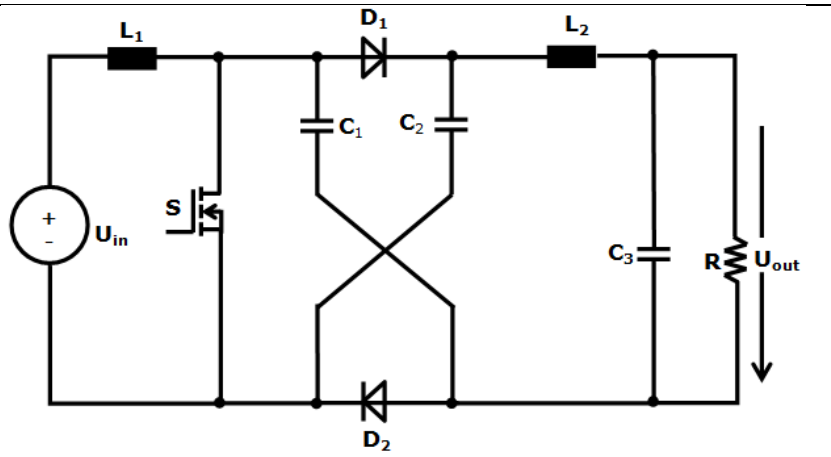
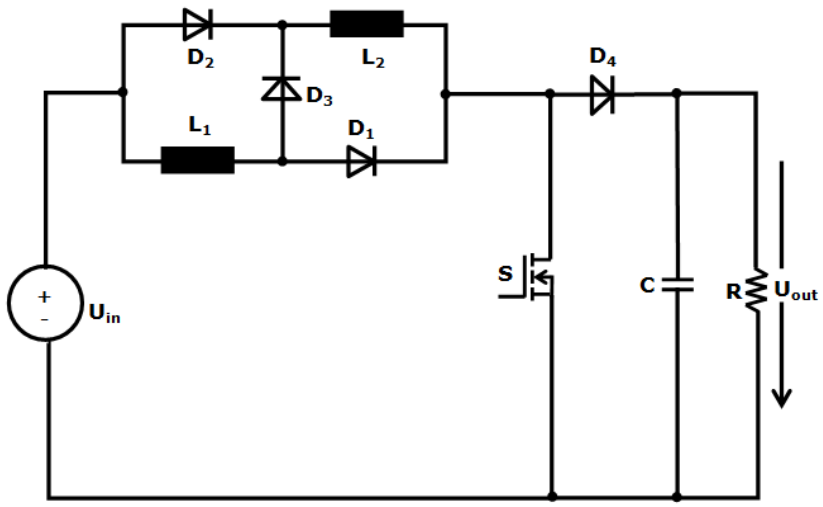
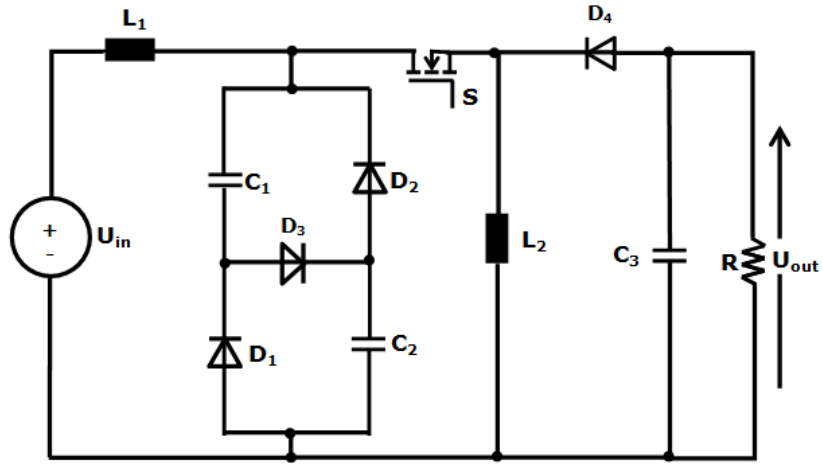
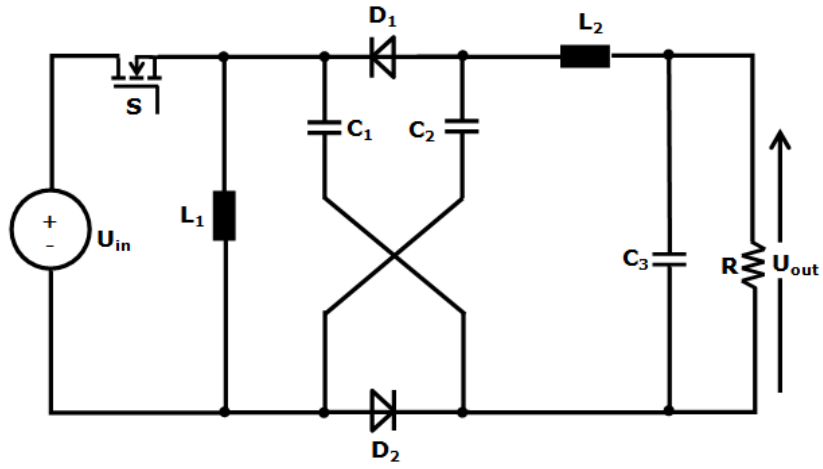
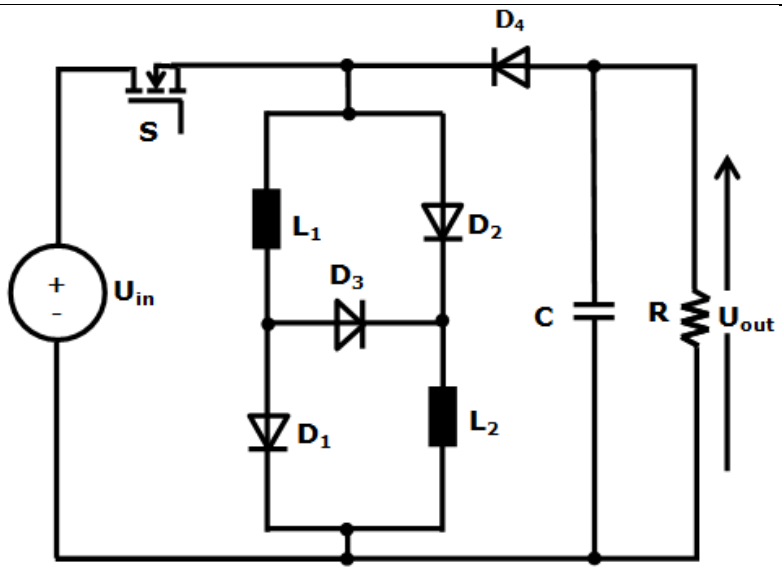
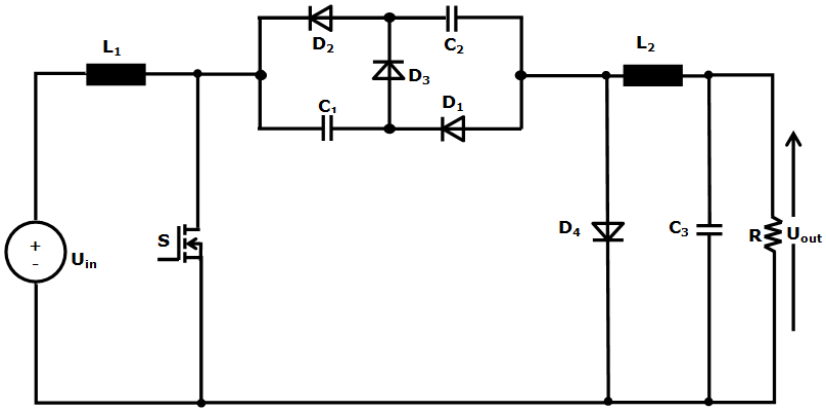
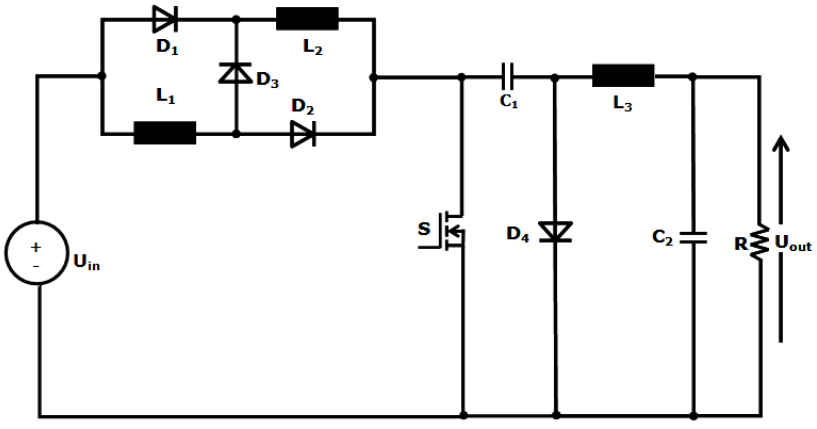
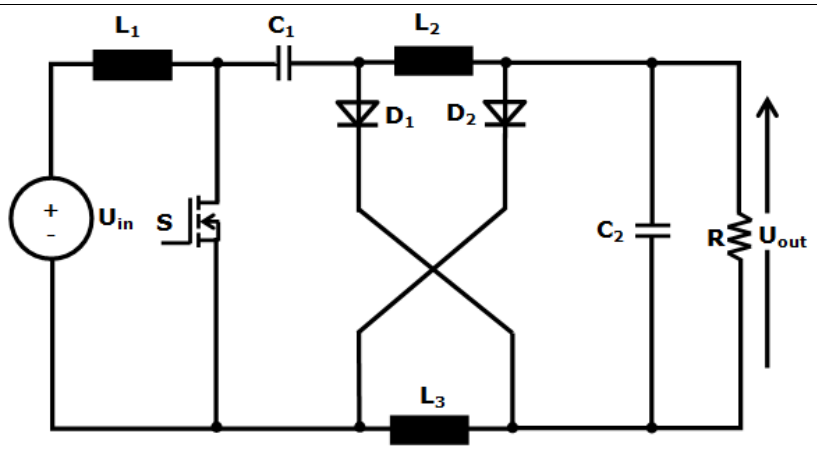
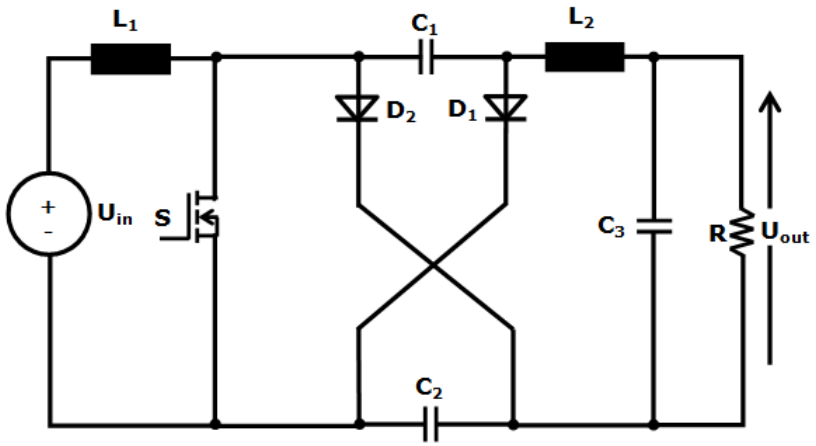
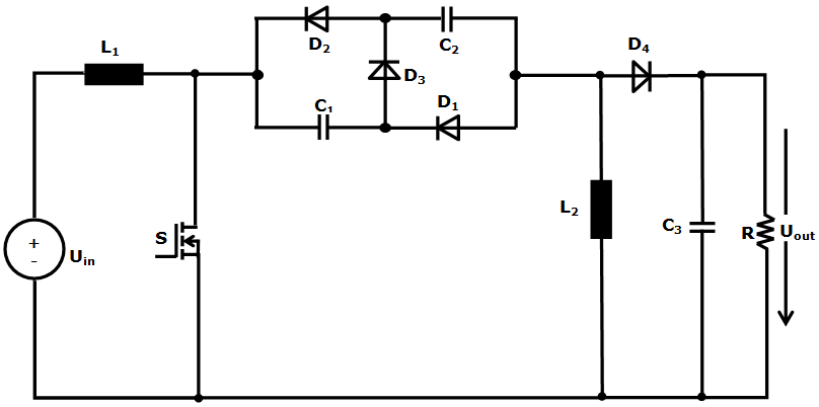
Switching structure name	Image of the switching structure
C-switching structures - Step-up 1	
C-switching structures - Step-up 2	
C-switching structures - Step-down 1	
L-switching structures - Step-down 1	
L-switching structures - Step-down 2	
L-switching structures - Step-up 1	

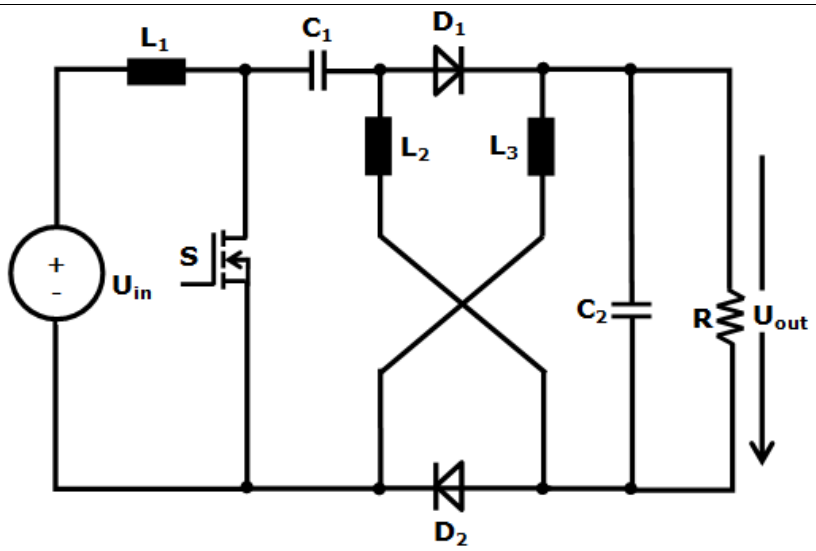
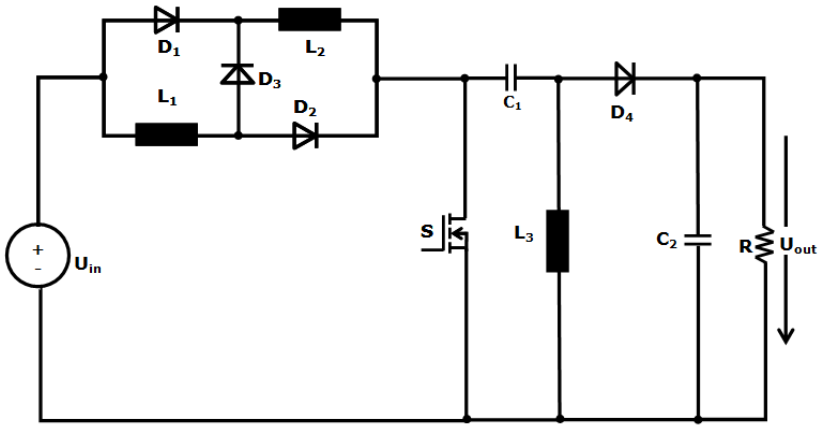
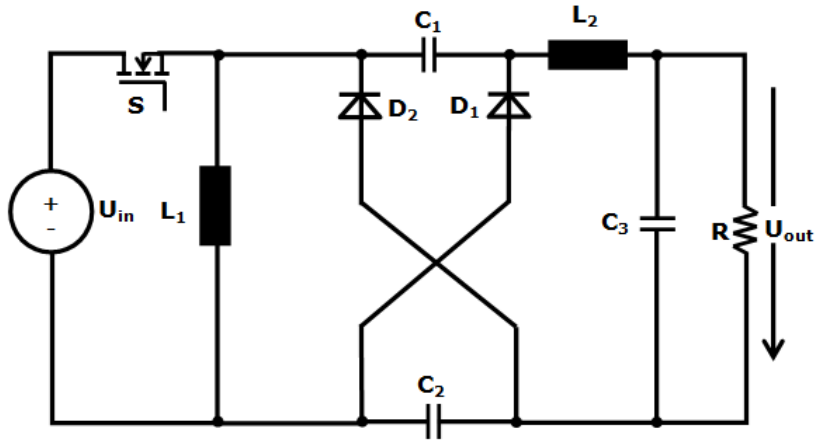
Table 1.3 Hybrid converters [1] - [5], [6], [7].

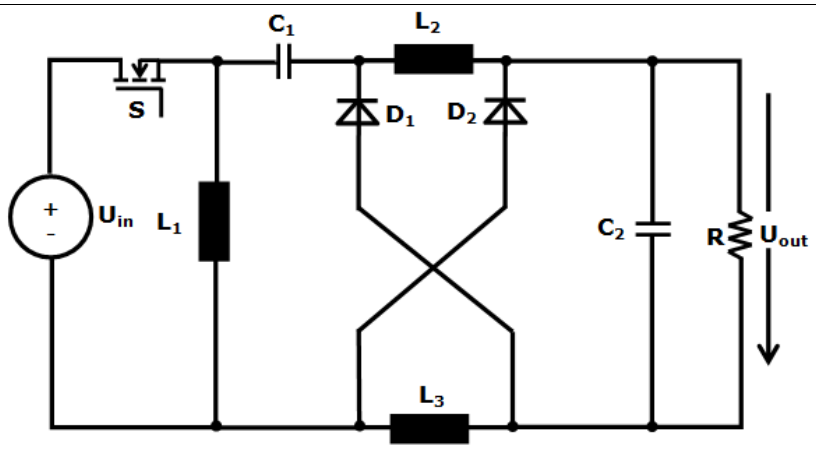
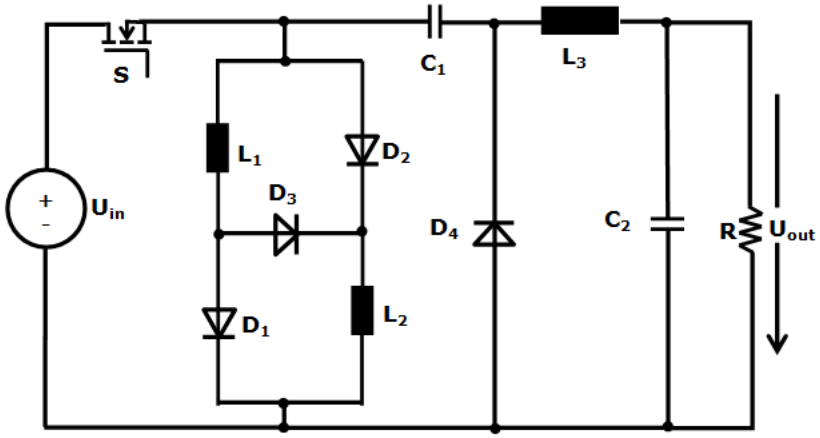
Converter name	Converter diagram	Static conversion ratio
1. Hybrid Buck converter with *C*-switching structure step-down 1		$M = \frac{d}{2-d}$
2. Hybrid Buck converter with *L*-switching structure step-down 1		$M = \frac{d}{2-d}$
3. Hybrid Boost converter with *C*-switching structure step-up 1		$M = \frac{1+d}{1-d}$

4. Hybrid Boost converter with *L*-switching structure step-up 1		$M = \frac{1+d}{1-d}$
5. Hybrid Buck-Boost converter with *C*-switching structure step-down 1		$M = \frac{d}{(1-d)\cdot(2-d)}$
6. Hybrid Buck-Boost converter with *C*-switching structure step-up 1		$M = \frac{2\cdot d}{1-d}$

7. Hybrid Buck-Boost converter with *L*-switching structure step-up 1		$M = \frac{2 \cdot d}{1 - d}$
8. Hybrid Ćuk converter with *C*-switching structure step-down 1		$M = \frac{d}{2 \cdot (1 - d)}$
9. Hybrid Ćuk converter with *L*-switching structure step-up 1		$M = \frac{(1 + d) \cdot d}{1 - d}$

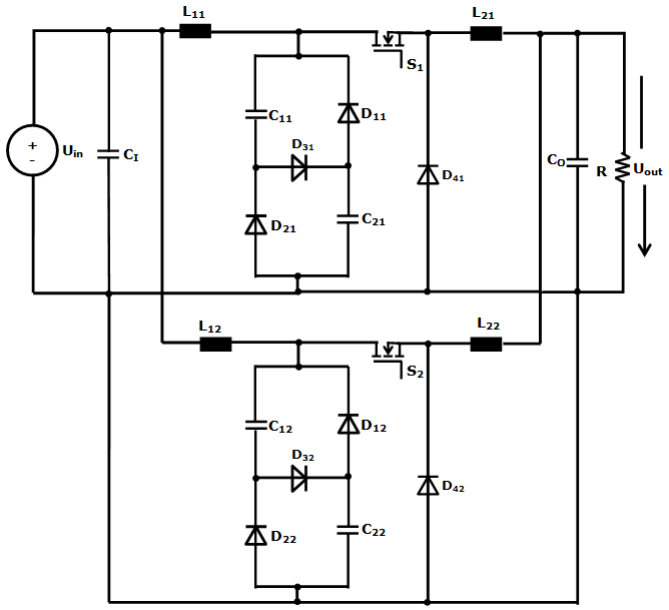
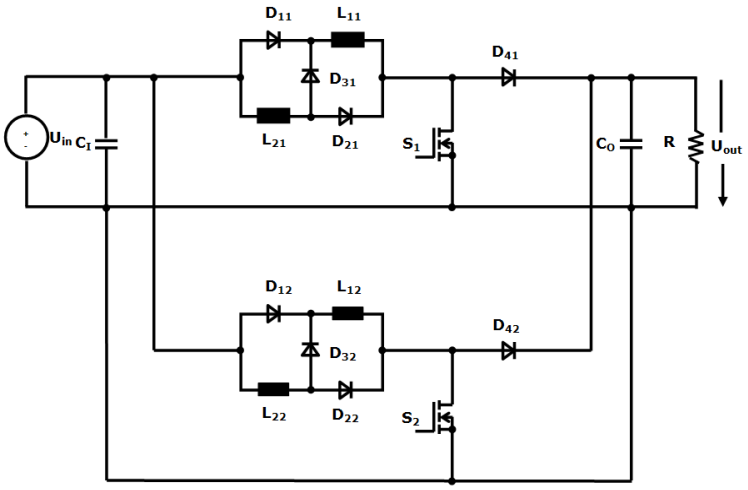
10. Hybrid Ćuk converter with *L*-switching structure step-down 1		$M = \frac{d}{2 \cdot (1-d)}$
11. Hybrid Ćuk converter with *C*-switching structure step-up 2		$M = \frac{1+d}{1-d}$
12. Hybrid Sepic converter with *C*-switching structure step-down 1		$M = \frac{d}{(1-d) \cdot (2-d)}$

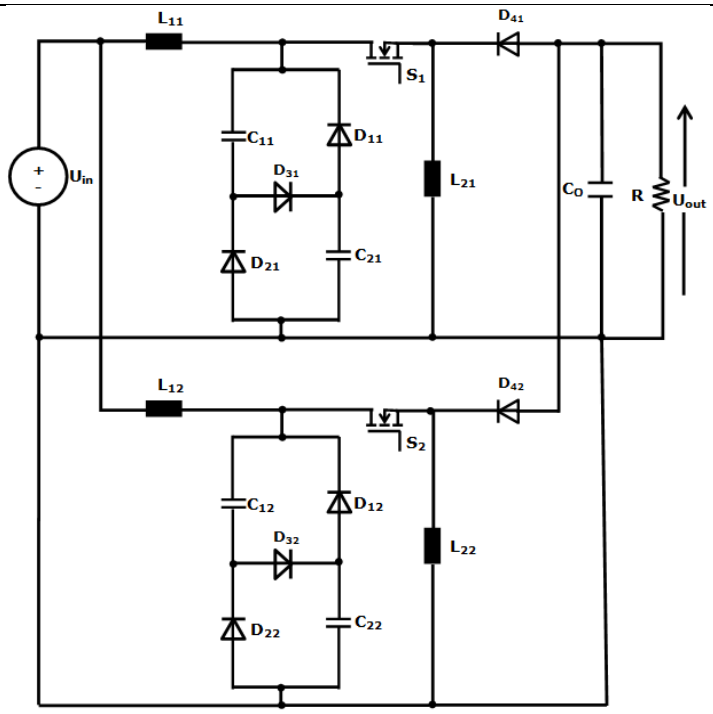
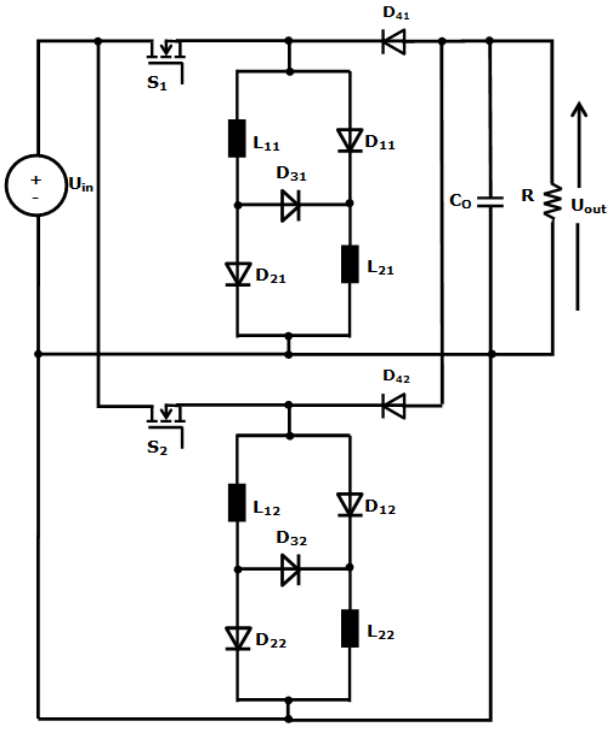
13. Hybrid Sepic converter with *L*-switching structure step-down 2		$M = \frac{d}{2 \cdot (1-d)}$
14. Hybrid Sepic converter with *L*-switching structure step-up 1		$M = \frac{(1+d) \cdot d}{1-d}$
15. Hybrid Zeta converter with *C*-switching structure step-up 2		$M = \frac{2 \cdot d}{1-d}$

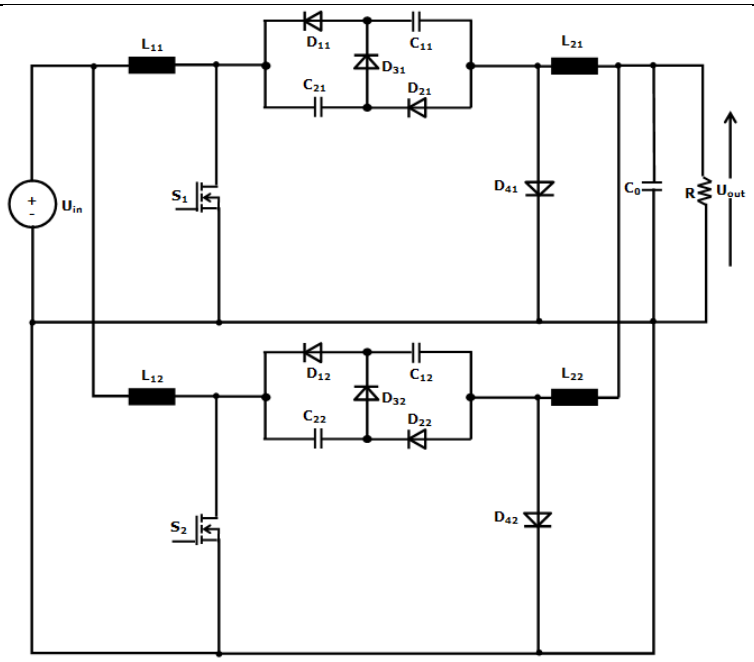
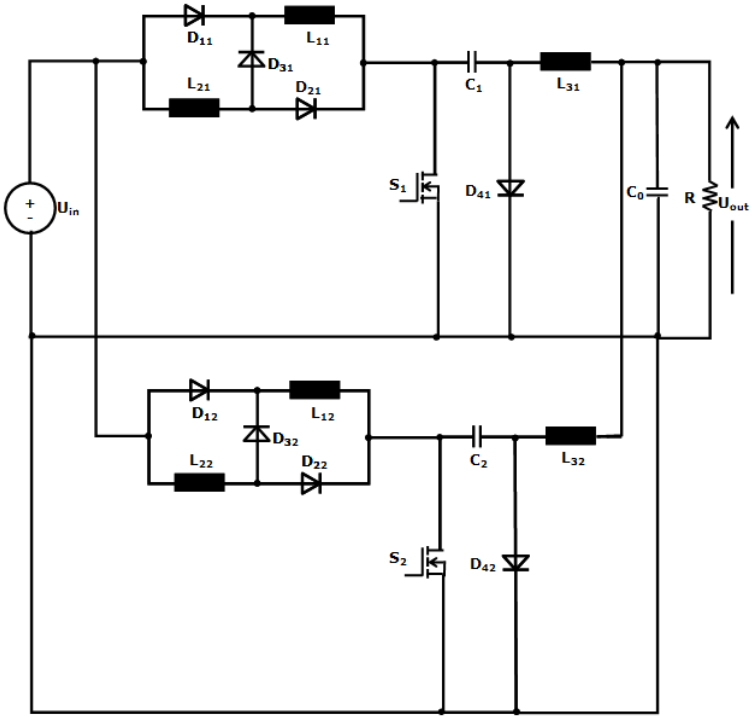
16. Hybrid Zeta converter with *L*-switching structure step-down 1		$M = \frac{d}{2 \cdot (1-d)}$
17. Hybrid Zeta converter with *L*-switching structure step-up 1		$M = \frac{(1+d) \cdot d}{1-d}$

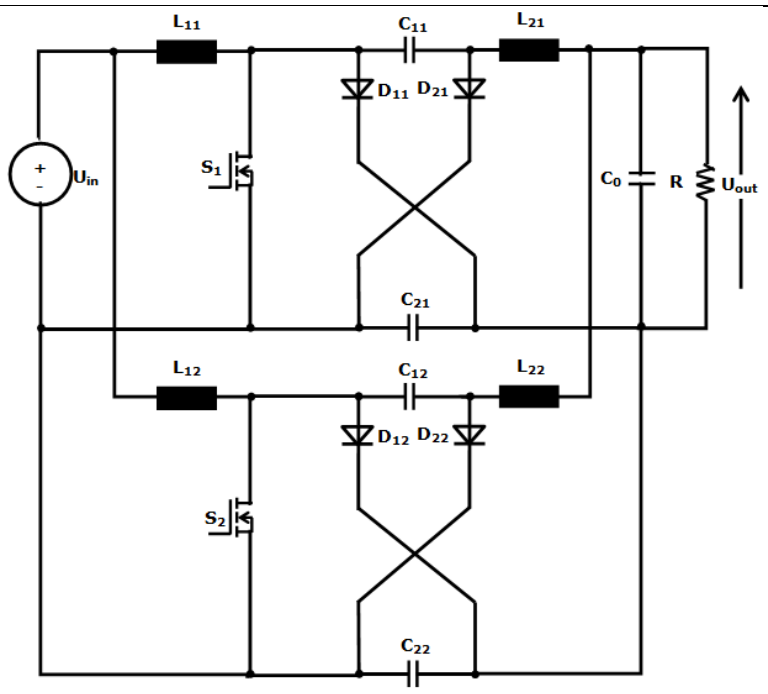
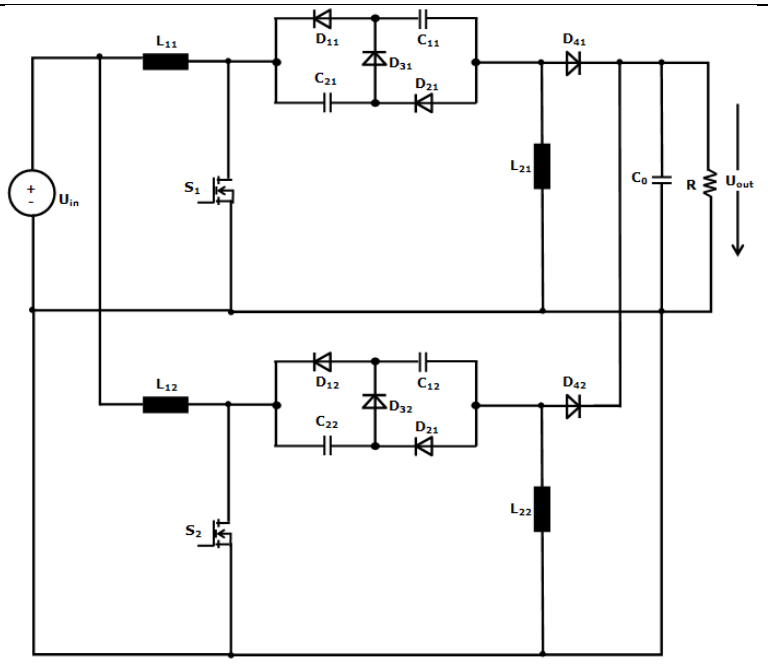
The second chapter of the PhD thesis continues with a comparative analysis in order to identify the most suitable hybrid converter for various applications. After the comparative analysis, from the examined converters in Table 1.3, 6 converters are selected, one generated by each switching cell and with the highest or lowest conversion ratio. Each selected converter is detailed with a circuit diagram, a brief circuit description, the dc output voltage formula, simulation waveforms, and an analysis of its advantages and disadvantages. This chapter end with a method for synthesizing multiphase hybrid converters, and the author proposes 11 new multiphase converters that are depicted in Table 1.4, together with their static conversion ratio.

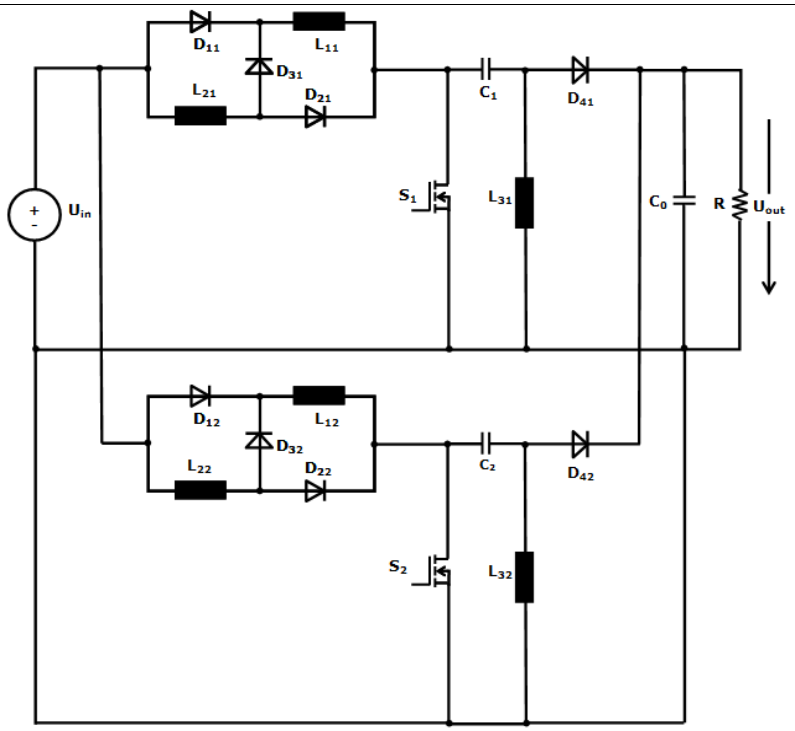
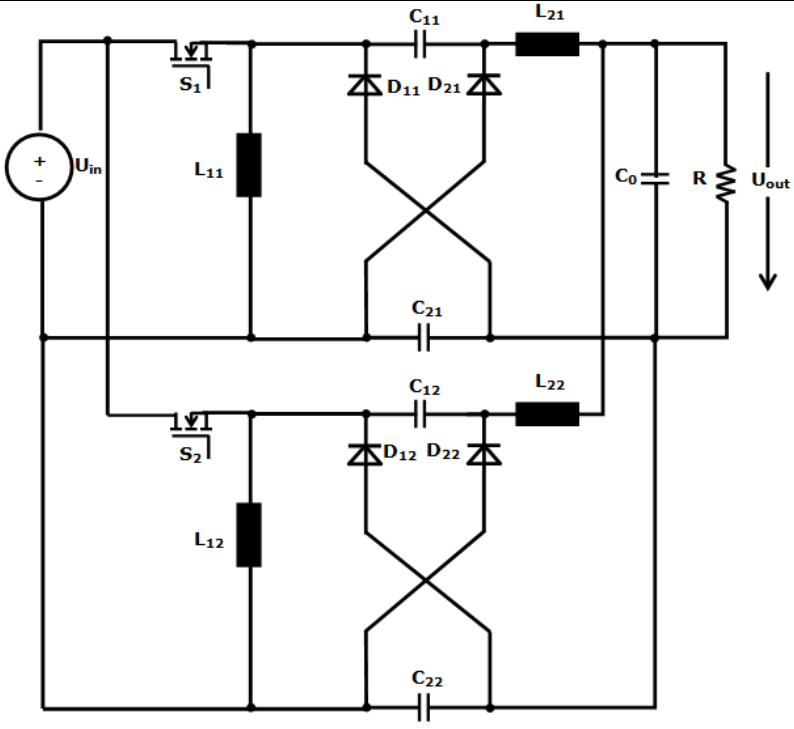
Table 1.4 Multiphase hybrid converters [1].

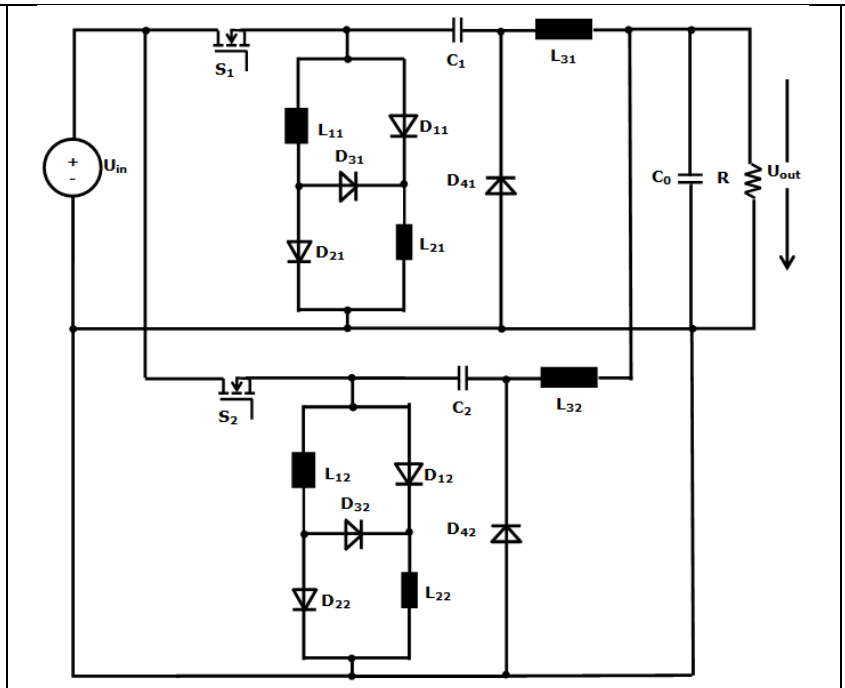
Converter name	Converter diagram	Static conversion ratio
1. Multiphase hybrid Buck converter with *C*-switching structure step-down 1		$M = \frac{d}{2-d}$
2. Multiphase hybrid Boost converter with *L*-switching structure step-up 1		$M = \frac{1+d}{1-d}$

3. Multiphase hybrid Buck-Boost converter with *C*-switching structure step-down 1		$M = \frac{d}{(1-d)\cdot(2-d)}$
4. Multiphase hybrid Buck-Boost converter with *L*-switching structure step-up 1		$M = \frac{2\cdot d}{1-d}$

5. Multiphase hybrid Ćuk converter with *C*-switching structure step-down 1		$M = \frac{d}{2 \cdot (1-d)}$
6. Multiphase hybrid Ćuk converter with *L*-switching structure step-up 1		$M = \frac{(1+d) \cdot d}{1-d}$

7. Multiphase hybrid Ćuk converter with *C*-switching structure step-up 2		$M = \frac{1+d}{1-d}$
8. Multiphase hybrid Sepic converter with *C*-switching structure step-down 1		$M = \frac{d}{(1-d)\cdot(2-d)}$

9. Multiphase hybrid Sepic converter with *L*-switching structure step-up 1		$M = \frac{(1+d)\cdot d}{1-d}$
10. Multiphase hybrid Zeta converter with *C*-switching structure step-up 2		$M = \frac{2\cdot d}{1-d}$

11. Multiphase hybrid Zeta converter with *L*-switching structure step-up 1		$M = \frac{(1+d)\cdot d}{1-d}$

Chapter 3 presents the hybrid Boost *L*-converter, focusing on analytical description, circuit waveforms and design guidelines. A comparative analysis between hybrid converters with coupled and uncoupled inductors was conducted, revealing that coupled inductors significantly reduce current ripple by half. This allows for lower switching frequency or smaller inductors, resulting in increased efficiency and reduced costs. To validate the theoretical findings, a single-phase Boost *L*-converter was designed and simulated in CASPOC, showing excellent agreement between simulation and theoretical calculations. A laboratory prototype was also built, and experimental results confirmed the theoretical considerations. The chapter concludes with efficiency diagrams comparing the prototype and Saber simulations for different output power level. The main contribution is the modification of the hybrid converter by using coupled inductors, resulting in a single core and reduced current ripple.

The hybrid multiphase Boost *L*-converter proposed by the author, in Chapter 4, was realized with the help of the step-up hybrid Boost *L*-converter discussed in Chapter 3 of the PhD thesis, now implemented in a multiphase design. By employing an interleaved switching strategy, the converter operates with all phases synchronized, but phase-shifted to improve performance. The analysis includes the theoretical relationships, waveforms sketches validated through simulations in the CASPOC program. The benefits of the multiphase configuration include improved input and output characteristics due to frequency multiplication, resulting in reduced filtering requirements and faster transient response. By coupling the inductors, the complexity of the circuit is reduced, the current ripple being half compared with the uncoupled case and minimizing the number of cores needed.

A comparison of coupled and uncoupled inductors versions shows that the coupled configuration is more efficient, and experimental results from a laboratory prototype validate the theoretical and simulated analyses. Despite the increased number of components in the two-phase design, it offers higher efficiency than the single-phase converter, reaching over 94% efficiency when the duty cycle is 1/3 and above 92% at 1/2. The chapter highlights the major advantages of

the multiphase hybrid converter and stresses the significance of this validation for the proposed family of converters. In the last chapter the conclusions and contributions of the PhD thesis are highlighted.

The author chose to begin with this presentation of the PhD research topic because part of the current research has its origins in the studies conducted during the PhD program.

The cooperation between Politehnica University of Timisoara and the University of Applied Science, Wilhelmshaven, played a pivotal role in the successful completion of the PhD research project. Under the expert supervision of Professor PhD. Eng. Viorel Popescu from the Applied Electronics Department at Politehnica University Timisoara, and the invaluable guidance of Professor PhD. Eng. Folker Renken during the research period abroad, the PhD project benefited from a blend of rigorous academic support and practical insights. The collaboration was further enriched by the technical assistance of Eng. Udo Schürmann, who offered his support for the building and testing the laboratory prototypes. This international partnership not only facilitated a comprehensive research experience but also fostered a remarkable learning environment which also led to future research.

2. Achievements in scientific, professional, and academic fields during post-doctoral period

2.1 Scientific research

This chapter presents a comprehensive summary of my research contributions after defending the PhD thesis entitled "A new class of high efficiency multiphase dc-dc converters", [1]. The PhD thesis was defended in 29.06.2015, at the Faculty of Electronics, Telecommunications and Information Technologies from Politehnica University of Timisoara. The Minister of National Education confirmed the PhD thesis through Order No. 4643, dated 30.07.2015.

My postdoctoral research has spanned several key areas, with a strong focus on the development [8]- [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], control [37], [38], [35], and applications like photovoltaic [19], [30] or fuel cell [39], [40], [41], [38] of DC-DC converters.

Although the most notable achievements are presented in distinct sections, reflecting original contributions to the field, there are instances where these sections overlap due to the interconnected nature of the research topics. This structure aims to highlight the depth of each area while also acknowledging the cross-disciplinary insights that have emerged from these overlapping contributions through the presentations of significant research projects and the most impactful publications in these areas conducting by the author.

2.1.1 New families of dc-dc converters

The discovery and development of new DC-DC converters is crucial due to their wide range of applications, including electronics (cellphones, laptops), automotive, renewable energy systems and DC grids. These converters must efficiently step-up, step-down, or both, depending on the input and output voltage requirements of each application. Innovative DC-DC converter topologies, such as quadratic, semiquadratic, hybrid or other advanced structures, offer improved efficiency, voltage gain, and reduced ripple, which are essential for optimizing energy used in renewable systems, like photovoltaic modules. Additionally, as renewable energy sources gain more importance in combating the energy and pollution crisis, enhanced DC-DC converters are necessary to maximize energy harvesting and integration into smart grids. Consequently, the discovery and development of new DC-DC converters are vital for advancing technology, improving energy efficiency, and supporting sustainable practices across various industries.

The contributions to the development of new converters are showcased in 28 papers and extensively covered by two major research projects, [42], [43]. The respective studies and projects have had a significant impact on expanding the knowledge and applicability of converters, addressing various technical challenges, and offering innovative solutions.

2.1.1.1 *Hybrid buck L DC-DC converter*

In the papers [8] - [9], a new two-phase hybrid Buck *L* converter is presented. Starting from the *L*-switching structure step-down 1 presented in [6], [7], [44], [45] - [46] and [1], replacing the diode *D* and the inductor *L* by the switching cell in the classical Buck, the converter described in [7] and [1] was developed. The circuit is presented in Figure 2.1.

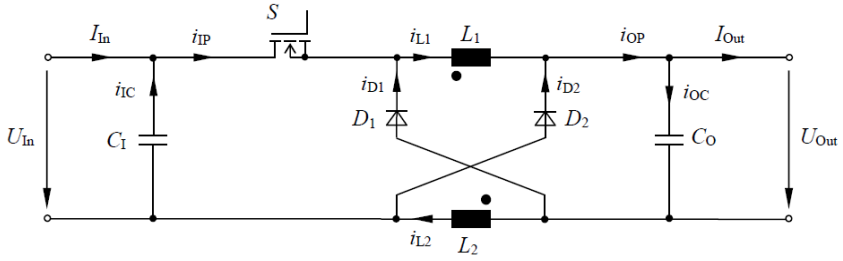


Figure 2.1 Single-phase hybrid buck *L* DC-DC converter.

In [8] and [9] the design of a multiphase hybrid Buck *L* converter is presented. All phases share a common input and output capacitor. The total current is distributed across multiple phases, which significantly reduces *AC* currents in both the input and output capacitors by employing an interleaved switching topology. Due to the presence of the main inductance in the negative rail of the converter, it is necessary to balance the current across the different phases. For this purpose, common-mode inductances, as shown in Figure 2.2 are placed in both the positive and negative rails of each phase.

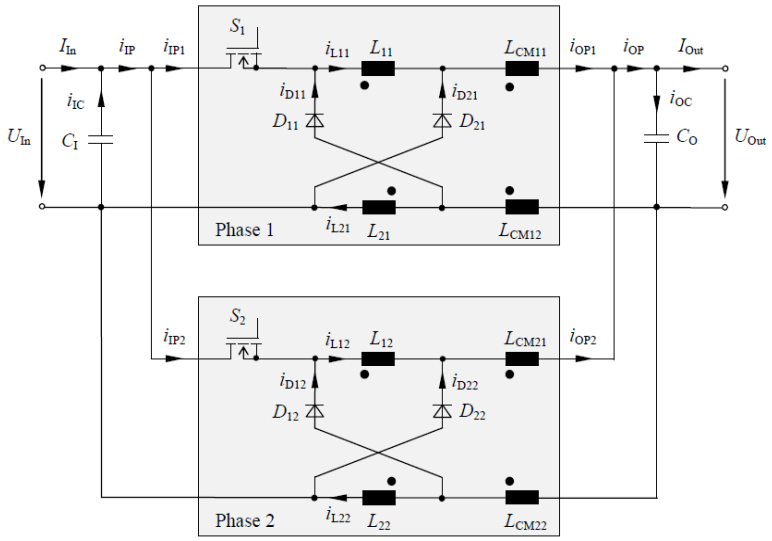


Figure 2.2 Two-phase interleaved hybrid buck *L* converter.

Additionally, this approach increases the frequency of the capacitor currents, leading to lower ripple effects. This configuration helps to maintain balance and optimizes performance in multiphase converter designs, effectively improving both efficiency and the overall operation of the system.

For the calculations, it is assumed that all converter components operate lossless, and that both input and output voltages together with the current are nearly *DC*. Additionally, the converter

is controlled via pulse width modulation, with switching states designated as t_{on} (on-state) and t_{off} (off-state).

The output voltage is:

$$U_{\text{Out}} = \frac{d}{2-d} \cdot U_{\text{In}} \qquad (2.1)$$

In comparison to the traditional buck converter, the hybrid buck *L* converter operate with a higher duty cycle for the same input and output voltage. A higher duty cycle indicates that the electronic switch is turned on for a longer amount of time. In the switched-on states of the hybrid buck *L* converter, energy is directly transferred from input to output. As a result, high efficiency with the same component effort is expected. The voltage ratio for both converters is plotted in Figure 2.3 as a function of duty cycle.

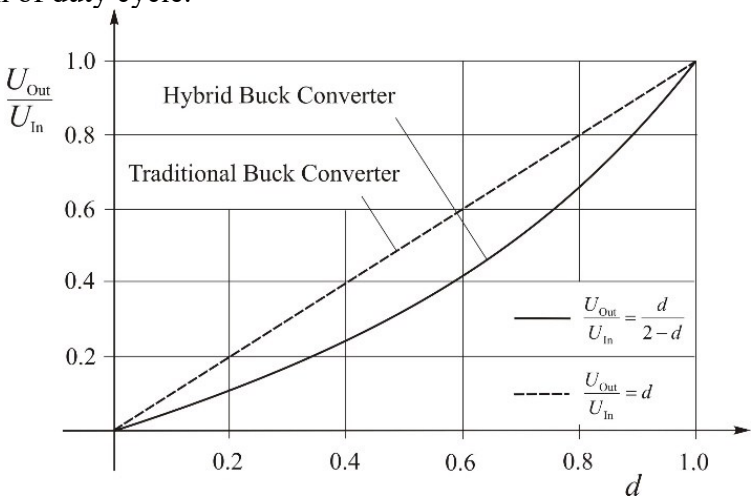


Figure 2.3 Voltage ratio of a traditional buck and a hybrid buck *L* converter.

Converter input circuit calculation

Figure 2.4 illustrates the input currents waveforms for a two-phase hybrid buck converter. The currents in both inductors, as well as the input current for phase 1, are displayed above, while the 2 phase currents are depicted below in green. The triangular-shaped inductor currents of the two phases are interleaved using a half period offset pulse. The input current of each phase are added resulting in a total input phase current (I_{IP}). It is assumed that only the *DC* component of the current flows through the circuit input. For multiphase converters, the relationship between the input current (I_{In}) and the average inductor current of the phases (I_{LnAV}) can be determined, [8] - [9] and [1].

$$I_{\text{Ln AV}} = \frac{I_{\text{In}}}{n \cdot d} \qquad (2.2)$$

The entire AC component of the input phase current, I_{IP}, equivalent to the input current, I_{IC}, is assumed to flow through the input capacitor.

The capacitors conduct the entire *AC* component of the input phase current, I_{IP}. This *AC* current is much lower than that of a single-phase hybrid buck-*L* converter, and the frequency of the capacitor current is also doubled, [8] - [9] and [1].

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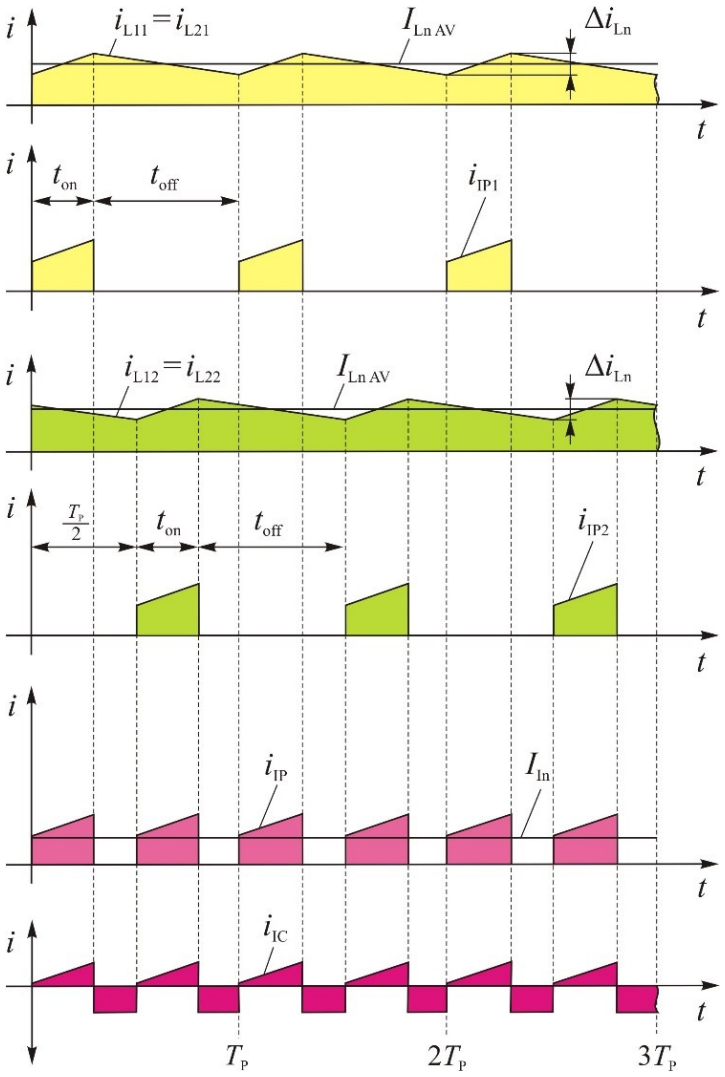

Figure 2.4 Input waveforms of a two-phase hybrid buck *L* converter (*d* = 0.3).

The calculation of circuit inductances in an *n*-phase design can be performed similarly to that of single-phase circuits. It is important to consider that the input current is distributed across the number of phases. Consequently, the maximum current variation in each individual inductance should be determined based on the maximum *DC* current at the rated power in the respective phases. Typically, for design purposes, the maximum current variation is chosen to range between 10% and 30% of the phase *DC* current in the inductances at rated power, [8] - [9] and [1].

.

$$L_{1n} = L_{2n} = \frac{U_{In} \cdot T_P}{\Delta i_{Ln\,max}} \cdot \left(3 - 2 \cdot \sqrt{2}\right) \qquad (2.3)$$

$$\Delta i_{Ln\,max} = (0.1 - 0.3) \cdot I_{Ln\,AV\,R} \qquad (2.4)$$

Since the amplitude of the triangular current variation in the inductors depends on the duty cycle of the converter, and the duty cycle remains the same across all phases, the current ripples in all inductors are identical, [8] - [9] and [1].

$$\Delta i_{\mathrm{Ln}} = \frac{(d)\cdot(1-d)}{(2-d)\cdot(3-2\cdot\sqrt{2})}\cdot \Delta i_{\mathrm{Lnmax}} \qquad (2.5)$$

In the calculation of the input capacitor for multiphase hybrid buck *L* converters, it is noted that, compared to a single-phase design, the capacitor current is reduced while the current frequency increases proportionally with the number of phases. The current in the capacitor is influenced by variations in the input voltage. Typically, for capacitor design, the allowable static voltage variation is chosen to be less than 1% of the rated input voltage, [8] - [9] and [1].

$$C_I = \frac{T_P \cdot I_{\mathrm{Ln\,AV}}}{4\cdot n\cdot \Delta u_{\mathrm{In\,max}}} \qquad (2.6)$$

$$\Delta \mathrm{u}_{\mathrm{In\,max}} \leq 0.01 \cdot \mathrm{u}_{\mathrm{In\,R}} \qquad (2.7)$$

For electrolytic capacitors, the RMS current load is a key design factor. To calculate the RMS current in the input capacitor I_C for multiphase DC-DC converters, ideal switching and *DC* input current are assumed. In the worst-case scenario, the capacitor handles the total *AC* current. The capacitor current consists of two components: a rectangular and a triangular part. The formula below shows the RMS current for the rectangular component in multiphase converters with *n* phases, [8] - [9] and [1].

$$I_{\mathrm{IC\ \Pi}} = \begin{cases} \sqrt{I_{\mathrm{Ln\,AV}}^2 \cdot n^2 \cdot \left(d-\frac{0}{n}\right)\cdot\left(\frac{1}{n}-d\right)} & \text{if } \frac{0}{n} \leq d \leq \frac{1}{n} \\ \sqrt{I_{\mathrm{Ln\,AV}}^2 \cdot n^2 \cdot \left(d-\frac{1}{n}\right)\cdot\left(\frac{2}{n}-d\right)} & \text{if } \frac{1}{n} \leq d \leq \frac{2}{n} \\ \sqrt{I_{\mathrm{Ln\,AV}}^2 \cdot n^2 \cdot \left(d-\frac{2}{n}\right)\cdot\left(\frac{3}{n}-d\right)} & \text{if } \frac{2}{n} \leq d \leq \frac{3}{n} \\ \bullet & \bullet \\ \bullet & \bullet \\ \bullet & \bullet \\ \sqrt{I_{\mathrm{Ln\,AV}}^2 \cdot n^2 \cdot \left(d-\frac{n-1}{n}\right)\cdot\left(\frac{n}{n}-d\right)} & \text{if } \frac{n-1}{n} \leq d \leq \frac{n}{n} \end{cases} \qquad (2.8)$$

As the number of phases increases, the average inductance current I_{LnAV} from formula (2.2) decreases. In a two-phase converter, I_{LnAV} is only half of that in a single-phase converter (see formula (2.2)), which reduces the rectangular component of the input capacitor current in a multiphase design. Additionally, the RMS current of the triangular components for multiphase converters with *n* phases is provided in the next formula.

$$I_{\mathrm{IC}\,\Delta} = \begin{cases} \sqrt{\Delta i^2_{\mathrm{Ln\,max}} \cdot \frac{n\cdot(1-d)^2\cdot\left[1^2\cdot\left(d-\frac{0}{n}\right)^3+0^2\cdot\left(\frac{1}{n}-d\right)^3\right]}{12\cdot(3-2\cdot\sqrt{2}\ \ )^2\cdot(2-d)^2}} & \text{if } \frac{0}{n}\le d\le\frac{1}{n} \\ \sqrt{\Delta i^2_{\mathrm{Ln\,max}} \cdot \frac{n\cdot(1-d)^2\cdot\left[2^2\cdot\left(d-\frac{1}{n}\right)^3+1^2\cdot\left(\frac{2}{n}-d\right)^3\right]}{12\cdot(3-2\cdot\sqrt{2}\ \ )^2\cdot(2-d)^2}} & \text{if } \frac{1}{n}\le d\le\frac{2}{n} \\ \sqrt{\Delta i^2_{\mathrm{Ln\,max}} \cdot \frac{n\cdot(1-d)^2\cdot\left[3^2\cdot\left(d-\frac{2}{n}\right)^3+2^2\cdot\left(\frac{3}{n}-d\right)^3\right]}{12\cdot(3-2\cdot\sqrt{2}\ \ )^2\cdot(2-d)^2}} & \text{if } \frac{2}{n}\le d\le\frac{3}{n} \\ \bullet\ \bullet\ \bullet & \bullet\ \bullet\ \bullet \\ \sqrt{\Delta i^2_{\mathrm{Ln\,max}} \cdot \frac{n\cdot(1-d)^2\cdot\left[n^2\cdot\left(d-\frac{n-1}{n}\right)^3+(n-1)^2\cdot\left(\frac{n}{n}-d\right)^3\right]}{12\cdot(3-2\cdot\sqrt{2}\ \ )^2\cdot(2-d)^2}} & \text{if } \frac{n-1}{n}\le d\le\frac{n}{n} \end{cases} \qquad (2.9)$$

The current variation $\Delta i_{\mathrm{Ln\,max}}$ from formula (2.4) is determined based on the rated average inductance current $I_{\mathrm{Ln\,AV}}$ during circuit design. As the number of phases increases, the current variation decreases. The total capacitor current in an *n*-phase hybrid buck *DC-DC* converter is the geometric combination of the RMS rectangular and triangular components, [8] - [9] and [1].

$$\mathrm{I_{IC}} = \sqrt{\mathrm{I^2_{IC\Pi}} + \mathrm{I^2_{IC\Delta}}} \qquad (2.10)$$

The results of the RMS current calculation for the input capacitor C_I in a multiphase *DC-DC* converter are shown in Figure 2.5. It can be observed that the capacitor's current load significantly decreases as the number of phases increases. The rectangular RMS component is the dominant factor, as indicated by the dotted lines where $\Delta i_{\mathrm{Ln\,max}} = 0$, [8] - [9] and [1].

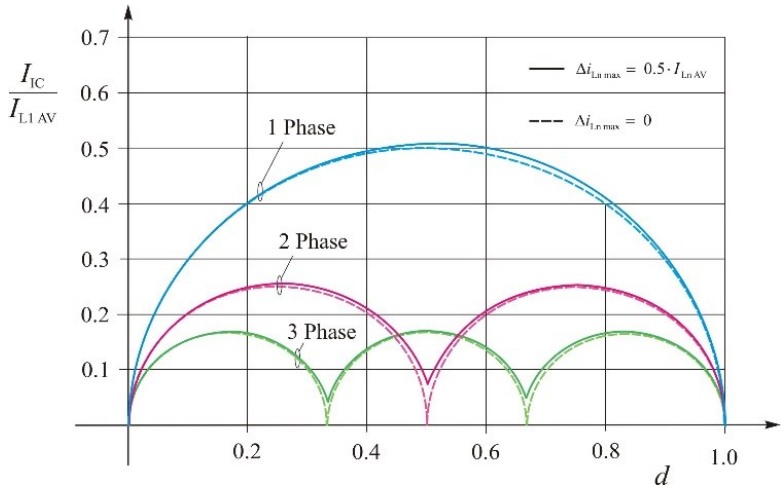

Figure 2.5 RMS-current in the input capacitors of a hybrid buck *L* converter.

In *n*-phase converters, the maximum capacitor current from the rectangular component decreases by a factor of *1/n*. The triangular current load is independent of the converted power and is determined by the inductance design. At rated output power, the rectangular component dominates, minimizing the triangular current's influence on the total capacitor current. The capacitor currents are shown with a variation of $\Delta i_{\mathrm{Ln\,N\,max}} = 0.5\, I_{\mathrm{Ln\,AV}}$, [8] - [9] and [1].

Converter output circuit calculation

Figure 2.6 illustrates the output current waveforms for a two-phase hybrid buck converter. The currents in both inductors, as well as the output current for phase 1, are displayed above, while the phase 2 currents are depicted below in green. The triangular-shaped inductor currents of the two phases are interleaved using a half-pulse period offset. During switched-on periods, the phase output currents are equal to the inductor currents. However, in the switched-off states, the output current of each phase is double that of the inductance current in a single-phase converter. The total output phase current I_{OP} is the sum of all phase output currents, as shown in the figure, along with the DC component I_{Out}, [8] - [9] and [1].

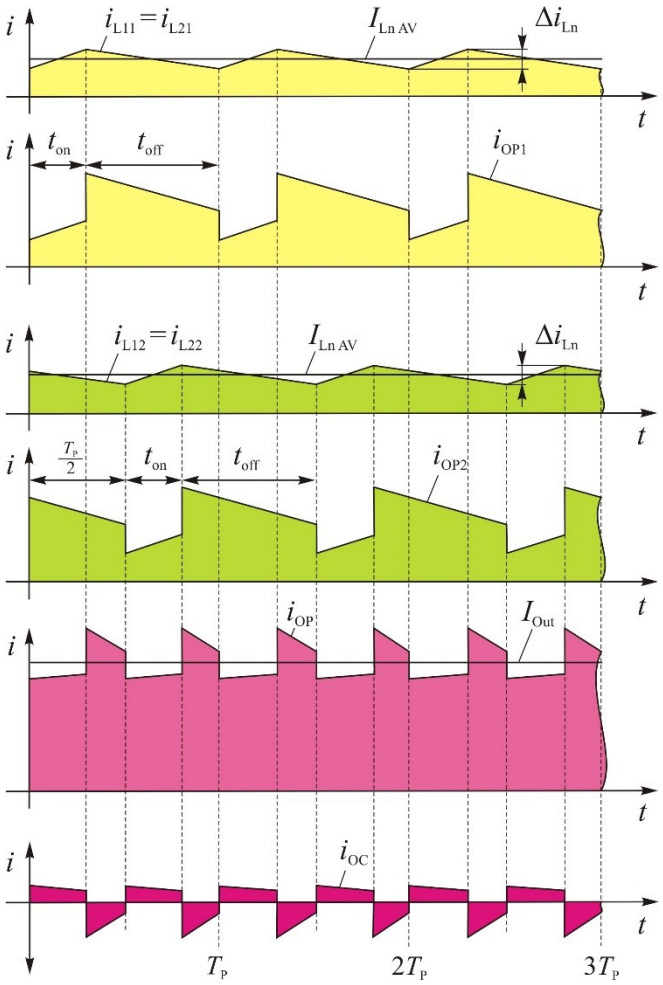

Figure 2.6 Output waveforms of a two-phase hybrid buck *L* converter ($d = 0.3$).

It is assumed that the *DC* current flows through the circuit's output, while the *AC* component of the overall output phase current I_{OP} flows through the output capacitor. This *AC*

current is significantly smaller, and its frequency is doubled compared to a single-phase buck converter. Similarly, for calculating the required output capacitance in a multiphase hybrid buck converter, the output capacitor current decreases while the current frequency increases with the number of phases. As a result, the capacitor current causes a voltage variation at the output. Typically, the permissible static voltage variation for capacitor design is set to be less than 1% of the rated output voltage, [8] - [9] and [1].

$$C_O = \frac{T_P \cdot I_{\text{Ln AV}}}{4 \cdot n \cdot \Delta u_{\text{Out max}}} \qquad (2.11)$$

$$\Delta u_{\text{Out max}} \leq 0.01 \cdot u_{\text{Out R}} \qquad (2.12)$$

The RMS current in the output capacitor C_O of the converter is calculated, and it can be divided into a rectangular and a triangular component. The formula below presents the RMS current of the rectangular part for multiphase converters with *n* phases, [8] - [9] and [1].

$$I_{\text{OC }\Pi} = \begin{cases} \sqrt{I_{\text{Ln AV}}^2 \cdot n^2 \cdot \left(d - \frac{0}{n}\right) \cdot \left(\frac{1}{n} - d\right)} & \text{if } \frac{0}{n} \leq d \leq \frac{1}{n} \\ \sqrt{I_{\text{Ln AV}}^2 \cdot n^2 \cdot \left(d - \frac{1}{n}\right) \cdot \left(\frac{2}{n} - d\right)} & \text{if } \frac{1}{n} \leq d \leq \frac{2}{n} \\ \sqrt{I_{\text{Ln AV}}^2 \cdot n^2 \cdot \left(d - \frac{2}{n}\right) \cdot \left(\frac{3}{n} - d\right)} & \text{if } \frac{2}{n} \leq d \leq \frac{3}{n} \\ \vdots & \vdots \\ \sqrt{I_{\text{Ln AV}}^2 \cdot n^2 \cdot \left(d - \frac{n-1}{n}\right) \cdot \left(\frac{n}{n} - d\right)} & \text{if } \frac{n-1}{n} \leq d \leq \frac{n}{n} \end{cases} \qquad (2.13)$$

The RMS current at the output capacitor produced by the triangular component in multiphase converters can be described by the following formula, [8] - [9] and [1]:

$$I_{\text{OC}\,\Delta} = \begin{cases} \sqrt{\Delta i^2_{\text{Ln max}} \cdot \frac{n\cdot\left[[1\cdot(d+1)-2nd]^2\cdot\left(d-\frac{0}{n}\right)^3+[0\cdot(d+1)-2nd]^2\cdot\left(\frac{1}{n}-d\right)^3\right]}{12\cdot(3-2\cdot\sqrt{2}\ \ )^2\cdot(2-d)^2}} & \text{if } \frac{0}{n}\le d\le\frac{1}{n} \\ \sqrt{\Delta i^2_{\text{Ln max}} \cdot \frac{n\cdot\left[[2\cdot(d+1)-2nd]^2\cdot\left(d-\frac{1}{n}\right)^3+[1\cdot(d+1)-2nd]^2\cdot\left(\frac{2}{n}-d\right)^3\right]}{12\cdot(3-2\cdot\sqrt{2}\ \ )^2\cdot(2-d)^2}} & \text{if } \frac{1}{n}\le d\le\frac{2}{n} \\ \sqrt{\Delta i^2_{\text{Ln max}} \cdot \frac{n\cdot\left[[3\cdot(d+1)-2nd]^2\cdot\left(d-\frac{2}{n}\right)^3+[2\cdot(d+1)-2nd]^2\cdot\left(\frac{3}{n}-d\right)^3\right]}{12\cdot(3-2\cdot\sqrt{2}\ \ )^2\cdot(2-d)^2}} & \text{if } \frac{2}{n}\le d\le\frac{3}{n} \\ \vdots & \vdots \\ \sqrt{\Delta i^2_{\text{Ln max}} \cdot \frac{n\cdot\left[[n\cdot(d+1)-2nd]^2\cdot\left(d-\frac{n-1}{n}\right)^3+[(n-1)\cdot(d+1)-2nd]^2\cdot\left(\frac{n}{n}-d\right)^3\right]}{12\cdot(3-2\cdot\sqrt{2}\ \ )^2\cdot(2-d)^2}} & \text{if } \frac{n-1}{n}\le d\le\frac{n}{n} \end{cases} \quad (2.14)$$

The rectangular component of the output capacitor's RMS current is identical to that of the input capacitor. Additionally, as the number of phases increases, the average inductance current I_{LnAV} from formula (2.2) decreases. The triangular RMS current component is independent of the converter load and is determined by the inductance design. For an *n*-phase converter, the total capacitor current is the geometric sum of the rectangular and triangular RMS components, as shown in the formula below, [8] - [9] and [1].

$$I_{\text{OC}} = \sqrt{I^2_{\text{OC}\Pi} + I^2_{\text{OC}\Delta}} \quad (2.15)$$

Figure 2.7 shows the total RMS current in the output capacitor C_{O} of a multiphase hybrid buck *L* converter. As the number of phases increases, the capacitor's current load decreases. The rectangular RMS component, which is the same in both input and output capacitors, dominates (see dotted lines, $\Delta i_{\text{Ln max}} = 0$). In *n*-phase converters, the maximum capacitor current from the rectangular part is reduced by a factor of *1/n,* [8] - [9] and [1].

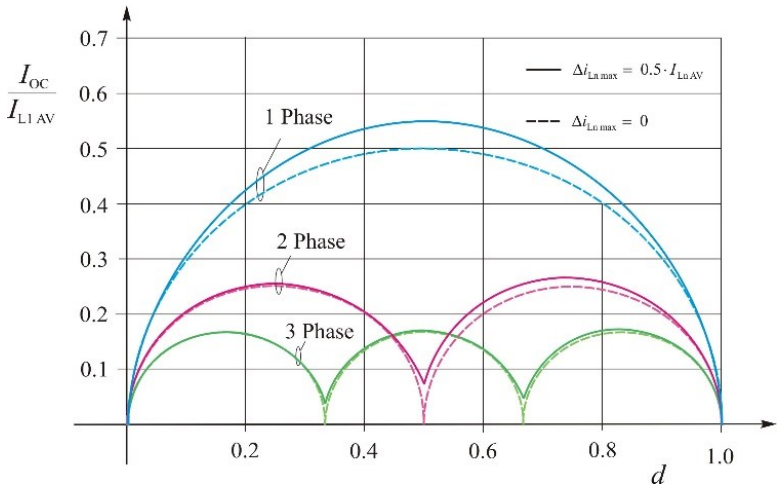

Figure 2.7 RMS-current in the output capacitors of a hybrid buck *L* converter.

The load on the output capacitors caused by the triangular current is independent of the converted power. At rated output power, this current has minimal impact on the overall capacitor current, represented by a variation of $\Delta i_{Ln\ N\ max} = 0.5\ I_{Ln\ AV}$. However, compared to the input capacitors, the triangular current has a greater influence on the output capacitors. In practice, the triangular current in the inductances can be increased because it has a limited effect on the total current in both input and output capacitors of multiphase converters. This allows for improved dynamics in the hybrid buck DC-DC converter and reduces the size of the inductances and capacitors required, [8] - [9] and [1].

In addition to the calculated current, harmonics from the switching processes also flow through the capacitors. These effects have been studied in other converters [47], and similar results can be applied to hybrid buck converters. At low loads, the additional current can significantly contribute to capacitor heating, while at higher output power, the calculated capacitor current dominates. However, this effect varies depending on the type of semiconductor and is influenced by the converter's switching frequency [9], [48] and [49].

Simulations of a hybrid Buck L converter

The simulations analyse the current waveforms of a two-phase hybrid Buck *L* converter using the CASPOC program, [50]. The converter circuit has an input voltage of 50V and a converter power of 400W. The pulse frequency of each phase is 50kHz, and the main inductance is in the minus line. A good, symmetrized current is achieved by common mode inductors L_{CM} = 2mH in each phase output. The simulation results, with a duty cycle of d=0.4 and d=2/3, are shown.

In Figure 2.8 and Figure 2.13, the inductor currents of the two-phase converter are presented. The four inductor currents have identical amplitudes, but the phase currents are shifted by half a pulse period. The switches in each phase are actuated with a half-pulse delay (Figure 2.9 and Figure 2.14). In switched-on states, the inductors are in series, meaning the inductor current also flows through the switches. At d=2/3, there is overlap in the current flow through the switches.

In switched-off states, the inductors are connected in parallel, and current flows through the diodes, with each diode handling the single inductor current (Figure 2.10 and Figure 2.15). The diode currents in different phases are time-shifted by half a pulse period, and at d=0.4, the current flows in the diodes overlap.

Figure 2.11 and Figure 2.16 show the input current I_{In} and the phase input current i_{IP} . During *ON*-state, the phase inductance current flows in the input phase, while the total input current remains constant. The difference between the input phase and input current is the input capacitor current. With d=0.4, there is no overlap in switch-on states, while at d=2/3, an overlap is observed. The average input current is I_{In} = 8A, leading to an input power of 400W.

Figure 2.12 and Figure 2.17 display the output phase current i_{OP} and the total output current I_{Out}. During switched-on states, the phase inductance current flows through the phase output, while during switched-off states, the output phase current is twice the inductance current. The total output current I_{Out} is nearly constant, with the output capacitor current being the difference between the output phase and total output current, [8] - [9] and [1].

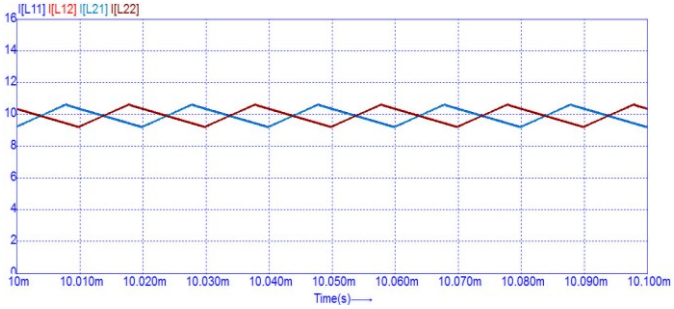

Figure 2.8 Inductor currents of a two-phase hybrid buck *L* converter (*d* =0.4).

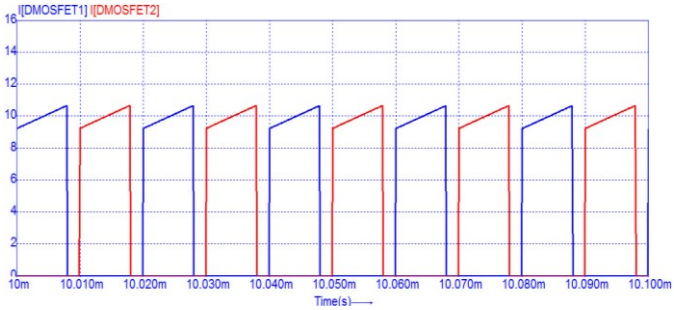

Figure 2.9 Switch currents of a two-phase hybrid buck *L* converter (*d* =0.4).

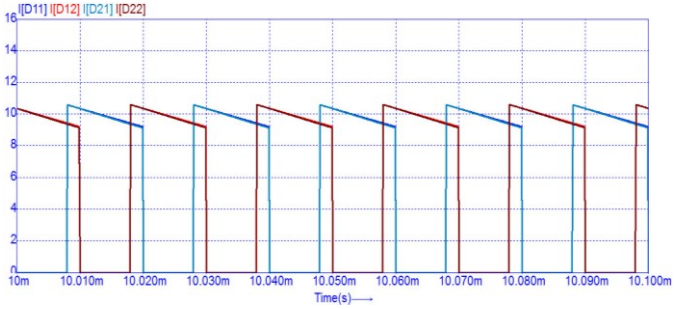

Figure 2.10 Diode currents of a two-phase hybrid buck *L* converter (*d* =0.4).

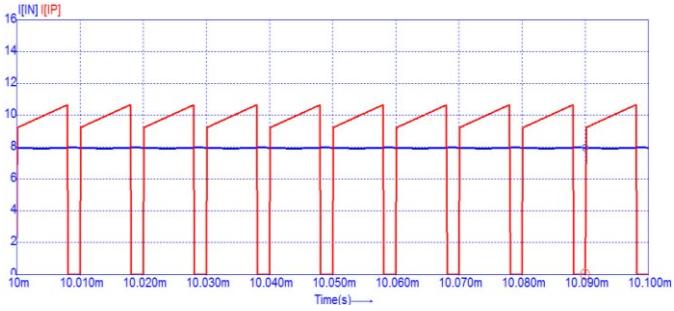

Figure 2.11 Currents at the input of a two-phase hybrid buck converter (*d* =0.4).

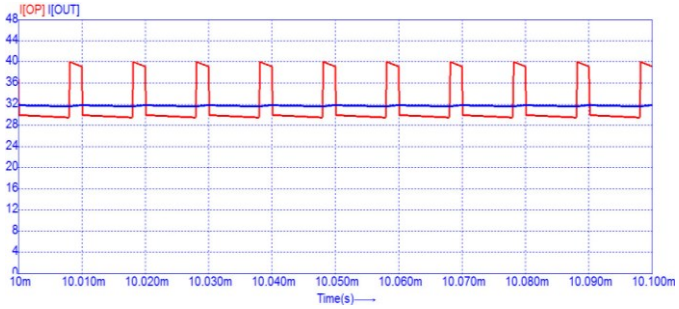

Figure 2.12 Currents at the output of a two-phase hybrid buck converter (d =0.4).

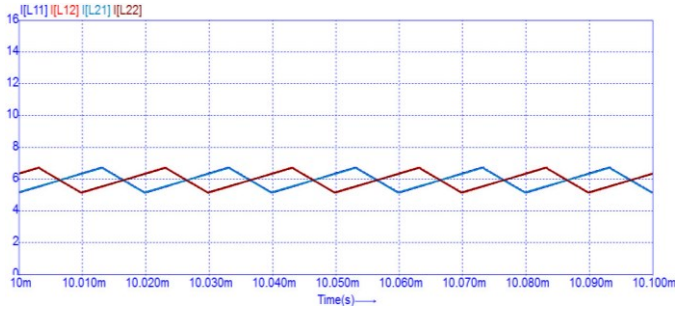

Figure 2.13 Inductor currents of a two-phase hybrid buck L converter (d =2/3).

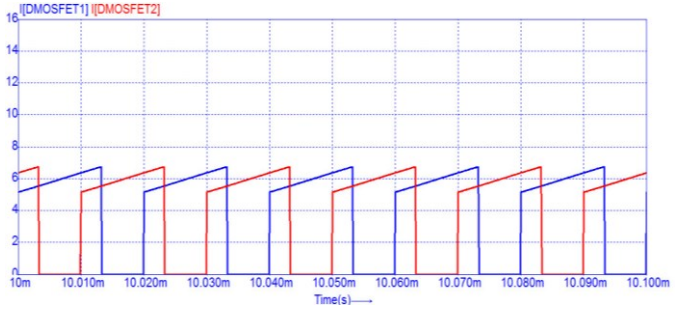

Figure 2.14 Switch currents of a two-phase hybrid buck L converter (d =2/3).

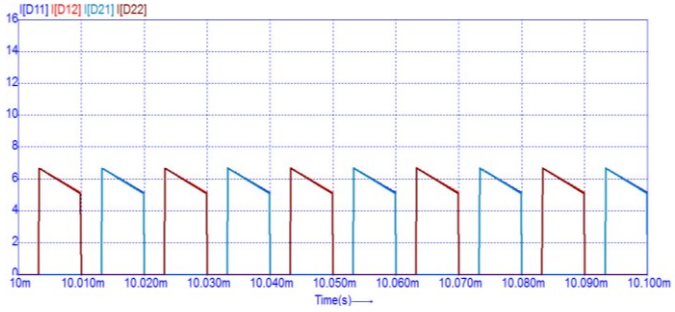

Figure 2.15 Diode currents of a two-phase hybrid buck L converter (d =2/3).

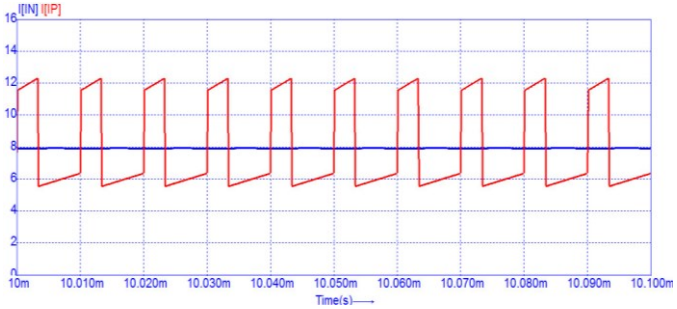

Figure 2.16 Currents at the input of a two-phase hybrid buck converter (d =2/3).

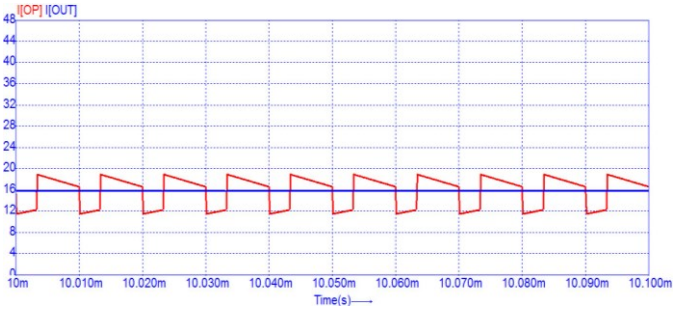

Figure 2.17 Currents at the output of a two-phase hybrid buck converter (d =2/3).

Can be remarked from Figure 2.12, that the diode currents of both phases overlap, causing the output phase current to be the sum of the double diode currents from both phases during those periods. In other periods, the output phase current is formed by the switch current of one phase and the double diode current of the other phase. The average output current is I_{Out} = 32A, with an output voltage of U_{Out} = 12.5V and output power of 400W.

In Figure 2.17 the switch currents of both phases overlap, making the output phase current, the sum of both switch currents during those periods. In other periods, the output phase current consists of the switch current from one phase and the double diode current from the other. In this case, the average phase output current is I_{Out} = 16A, with an output voltage of U_{Out} = 25V, still achieving the same output power of 400W.

In the paper [8], the two-phase hybrid Buck L converter is compared with the single-phase Buck-L converter. In each case the input voltage: U_{IN} = 50V and the rated power of the converters P_{Out} = 300W. The pulse frequency of the converter f_P = 50kHz and the duty cycle d = 0.5. The current in the inductors i_{L1} and i_{L2} are shown in the Figure 2.18, for a single-phase hybrid Buck-L converter.

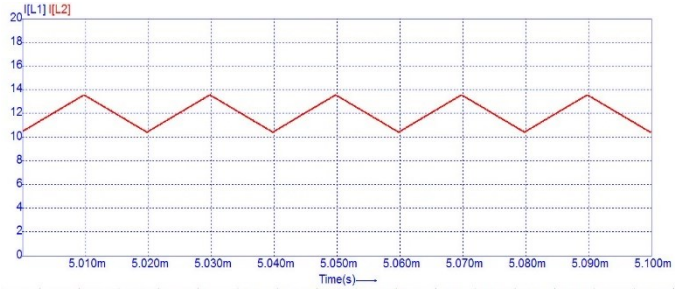

Figure 2.18 Inductor currents of a single-phase hybrid buck L converter.

In Figure 2.19, the input phase current i_{IP} and converter input current I_{In} are shown. When switched on, the input phase current equals the inductor current, and in the off state, it drops to zero. The difference between these is the input capacitor current.

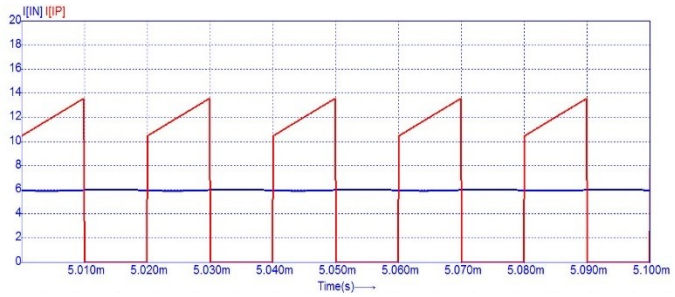

Figure 2.19 Currents at the input of a single-phase hybrid buck *L* converter.

Figure 2.20, shows the output phase current i_{OP} and output current I_{Out}. When switched on, the output phase current matches the inductor current, while during the off state, it doubles. The output current I_{Out} remains nearly constant, with the difference being the output capacitor current.

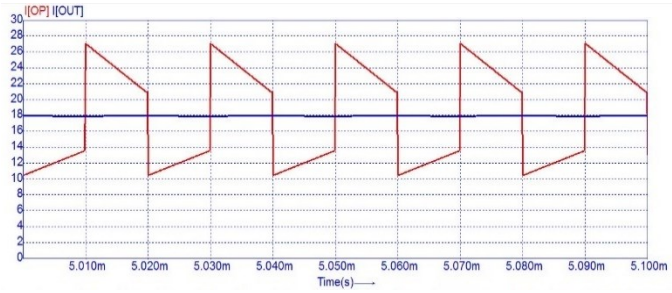

Figure 2.20 Currents at the output of a single-phase hybrid buck *L* converter.

In these examples, the input current I_{In} and output current I_{Out} remain nearly constant. This situation represents the worst-case scenario for sizing the filter capacitors and calculating the RMS current, as in this case, all the *AC* current components flow through the capacitors, [8] - [9] and [1].

For comparison, simulations were performed on the two-phase hybrid Buck *L* converter, with the current names as shown in the figures bellow. The pulse frequency for each phase is f_P = 50kHz, and the duty cycle is d = 0.5. The inductor currents in the two-phase converter, shown in the Figure 2.21, have the same amplitude but are phase-shifted by half a pulse period.
Figure 2.22, illustrates the input current I_{In} and the input phase current i_{IP}. During the *ON*-state of a switch, the corresponding inductor phase current flows through the input phase i_{IP} , with no overlap or current gaps at d = 0.5. The input current I_{Int} remains constant, and the difference between the input phase current and input current is the input capacitor current, which is significantly lower compared to a single-phase converter. At this duty cycle, the input capacitor current reaches a minimum (see Figure 2.5).
In Figure 2.23, the output phase current i_{OP} and converter output current I_{Out} are shown. During the *ON*-state, the inductor current flows through the output phase. When switched *off*, the output

phase current is twice as large as the inductor current. With $d = 0.5$, one phase is *ON* while the other is *OFF*, making the output phase current i_{OP} roughly three times higher than the inductor current. The output current I_{Out} is nearly constant, and the output capacitor current, similar to the input capacitor current, is significantly lower than in a single-phase converter, reaching a minimum at this duty cycle (see Figure 2.7).
In this simulation, both the input I_{In} and output I_{Out} currents are nearly constant, which represents the worst case for calculating the filter capacitors and the RMS capacitor current.

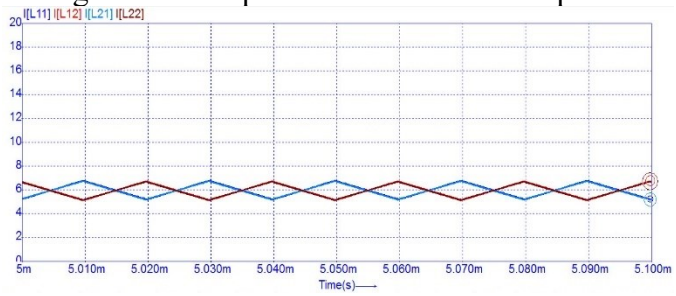

Figure 2.21 Inductor currents of a two-phase hybrid buck *L* converter.

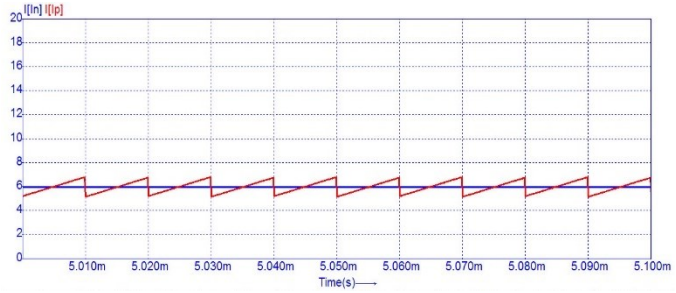

Figure 2.22 Currents at the input of a two-phase hybrid buck *L* converter.

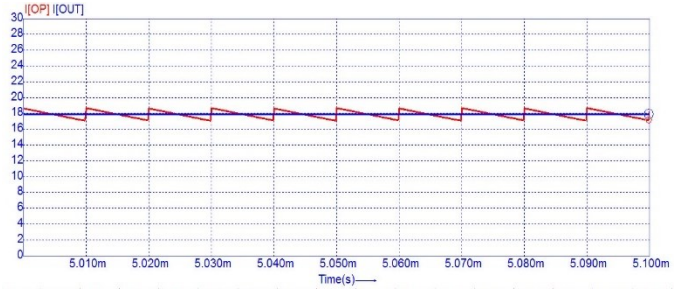

Figure 2.23 Currents at the output of a two-phase hybrid buck *L* converter.

In the two-phase converter circuit, the inductance currents in both the positive and negative lines of each phase are nearly identical (see Figure 2.21). This balanced current is achieved using large common mode inductors in the phase outputs (L_{CM} = 2mH). Simulations are now used to determine the required values for these common mode inductors in the circuit.
The next figure shows the inductance currents when smaller common mode inductors (L_{CM} = 0.5mH) are used. In this case, the phase currents are not sufficiently balanced, causing the current in the negative line to be slightly lower than in the positive line. When phase currents become more asymmetrical, it can alter the converter's voltage ratio, leading to unstable operating conditions, which should be avoided, [8] - [9] and [1].

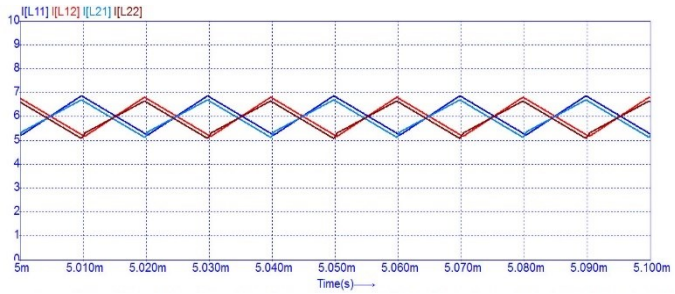

Figure 2.24 Inductor currents in case of reduced common mode inductors.

The two common mode inductors must compensate as much imbalance as possible. Any residual inductance in the output circuit can lead to significant oscillations, complicating the practical implementation of the circuit design.

Alternatively, double pole switches can be used instead of common mode inductors to achieve current symmetry between the phases. In this approach, the two switches from the respective phases must always switch simultaneously to maintain balanced phase currents.

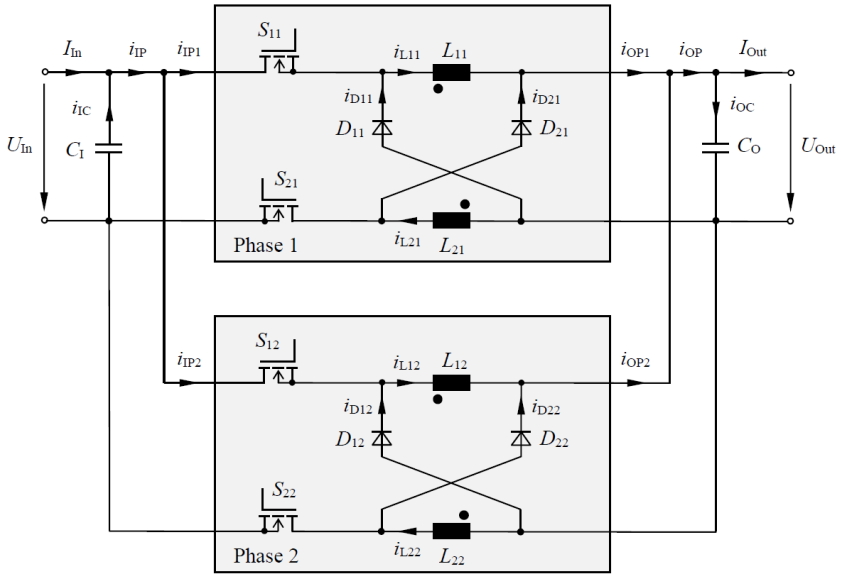

Figure 2.25 Design of a two-phase converter with bipolar switches.

Figure 2.26 displays the waveforms of the four inductor currents in a two-phase converter with a duty cycle of $d = 0.5$. The currents in the two individual phases are identical, indicating balanced operation across the phases.

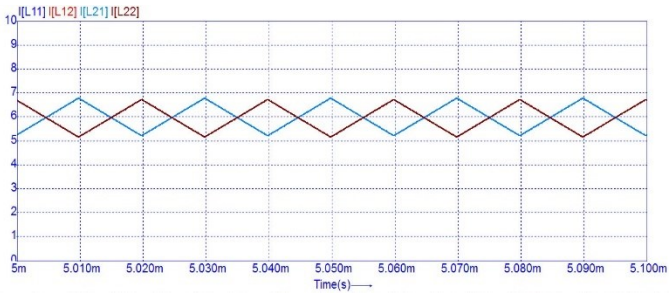

Figure 2.26 Inductor currents in the circuit with bipolar switches (d = 0.5).

In the illustrated inductor current waveforms, only one bipolar switch is turned on at a time. However, studies have shown that this method also functions effectively with overlapping switching durations between different phases, achieving good current balancing. The downside of this approach is that the converter experiences slightly higher losses due to the use of bipolar switches, [8] - [9] and [1].

In multiphase configurations, current balancing between phases is necessary, requiring additional components like common mode inductors presented in the paper [8] - [9]. However, incomplete compensation can cause oscillations. In simulations was also tested double pole switches, which improved current balancing but slightly increased losses. Overall, the added complexity for balancing currents is difficult to justify, even with the advantages of multiphase designs.

The design incorporating common mode inductors was selected for the practical implementation of the Hybrid Buck *L* Converter, and the results will be compared with both simulations and the theoretical analysis.

Practical performance evaluation of a hybrid Buck L converter

In this section, the calculated and simulated currents are compared with practical measurements from a two-phase hybrid buck *L* converter. Figure 2.27, shows the implemented converter, with a maximum power output 400W and a pulse frequency of 50kHz for each phase.

In the circuit, the inductor coils of the phases are coupled to reduce the overall inductance requirements. Loops are included in the inductor connections for easier current measurements. Small current transformers are used to measure currents in the semiconductor components.

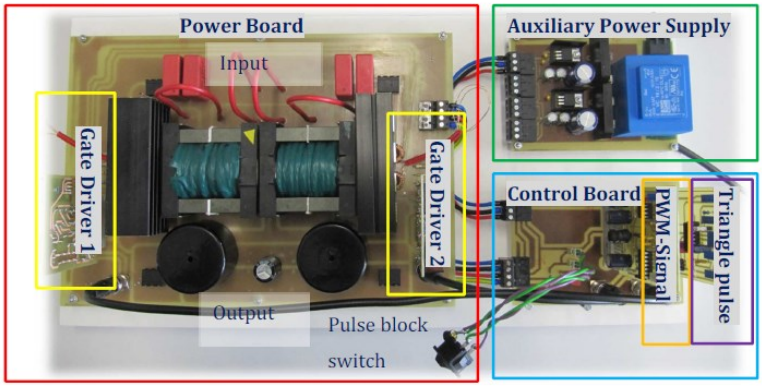

Figure 2.27 Realized hybrid buck *L* converter with output power of 400W.

Since the main inductance is located in the negative line of the circuit, the phase currents need to be balanced using common mode inductors at the phase outputs. Two common mode inductors with values of L_{CM} = 2mH are used to achieve maximum compensation. Any residual inductance in the output circuit could cause significant oscillations, making the practical implementation of the design more challenging.

To control the power unit, two PWM signals shifted by half a pulse period are required. This is achieved by comparing a triangular *AC* voltage with positive and negative *DC* voltages. The triangular voltage has a constant maximum value and a frequency matching the converter's phase pulse frequency. The two *DC* voltages are equal in magnitude and adjustable, generating the two PWM signals shifted by half a pulse period. The pulse widths of both signals can be simultaneously adjusted by varying the *DC* voltages.

Figure 2.28 shows the triangular *AC* voltage alongside one of the *DC* voltages. The level of the second *DC* voltage is also indicated. Both *DC* voltages can be adjusted between the maximum and minimum values of the triangular voltage, allowing for control of the PWM signals, [8] - [9] and [1].

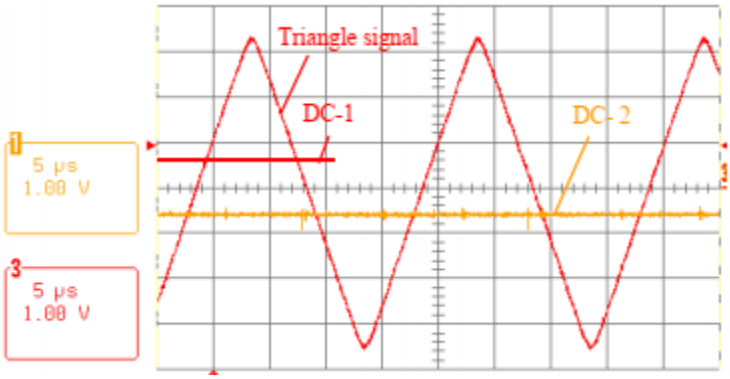

Figure 2.28 Generating of the PWM-signals.

Figure 2.29 and Figure 2.30 display the PWM signals for the electronic switches in both phases. The duty cycle of the control signals is identical for both phases. In Figure 2.29, the duty cycle is *d*=0.4, while in Figure 2.30, the duty cycle is increased to *d*=2/3 by adjusting the *DC* voltages.

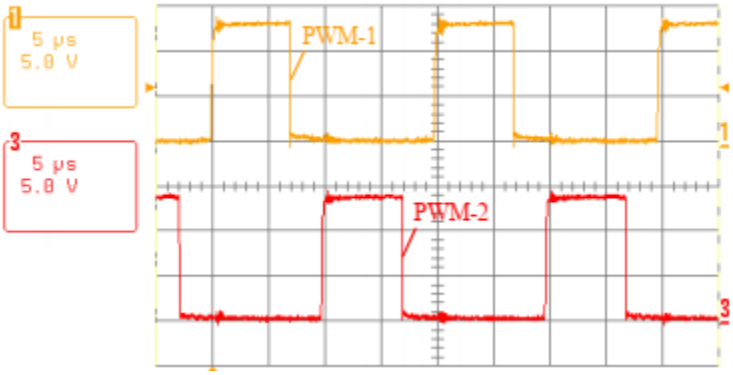

Figure 2.29 PWM-signals with a duty cycle d = 0.4.

The two PWM signals control the electronic switches of the power unit, with gate drivers ensuring proper phase-shifted control of the power semiconductors. Next, measurements of the converter's

power unit are shown. The current in the power semiconductors is measured using small current transformers with a transformer ratio of 1/50.
Figure 2.31 presents the measured current waveforms, with the duty cycle approximately $d \approx 2/3$ and the output power around $P_{OUT} \approx 150$W. At this operating point, the electronic switches have overlapping on-times. Since the current transformers only measure *AC* components, the zero line is marked in the figure. The principal current waveforms match the simulation results shown in previous figures.

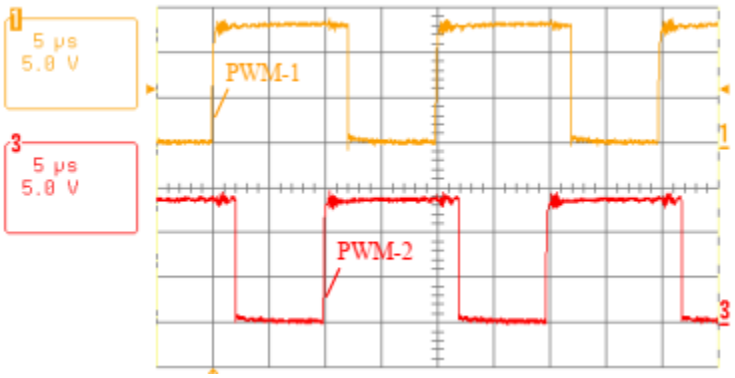

Figure 2.30 PWM-signals with a duty cycle $d = 2/3$.

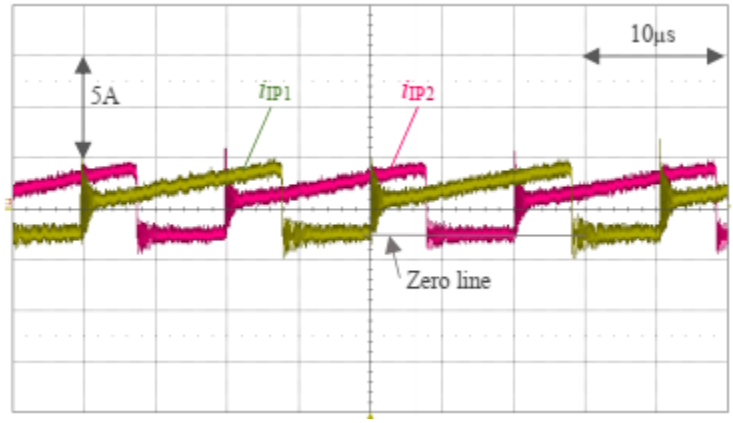

Figure 2.31 Current in the MOSFETs with a duty cycle $d = 2/3$.

In the switched-*off* state, the inductor current continues to flow through the diodes. This is clearly shown in Figure 2.32, where the current in the MOSFET stops, and the diode current starts to flow. The corresponding waveforms are also reflected in the simulation results shown in Figure 2.15.

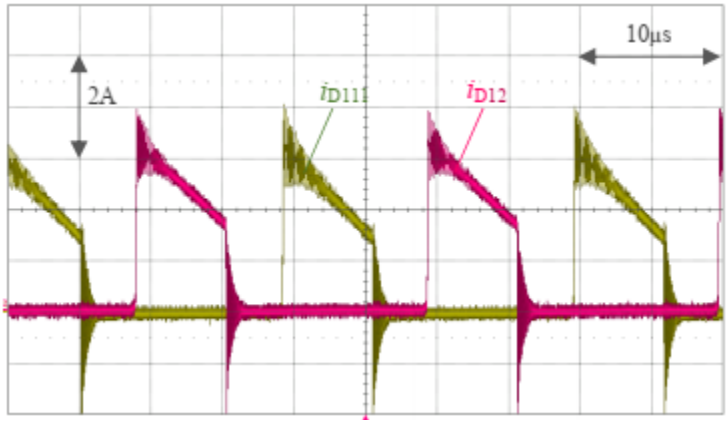

Figure 2.32 Current in the diodes with a duty cycle $d \approx 2/3$.

The practical current waveforms closely match the simulated and mathematically calculated results. The use of a multi-phase structure significantly reduces the currents in the input and output capacitors, lowering the filtering requirements. However, to balance the currents across phases, common mode inductors are necessary in each phase. While this method achieves good balancing, it slightly increases circuit losses.

Finally, efficiency curves for the hybrid buck converter were determined by measuring the input and output power. Efficiency was calculated across a range of output powers from P_{OUT} = 20W to 400W, with a consistent output voltage of U_{OUT} = 24V and input voltage of 50V. The efficiency of the practical hybrid buck L converter is shown in Figure 2.33. The maximum efficiency is approximately 95% at an output power of 70W, while the efficiency at the rated output power is around 87%, [8] - [9] and [1].

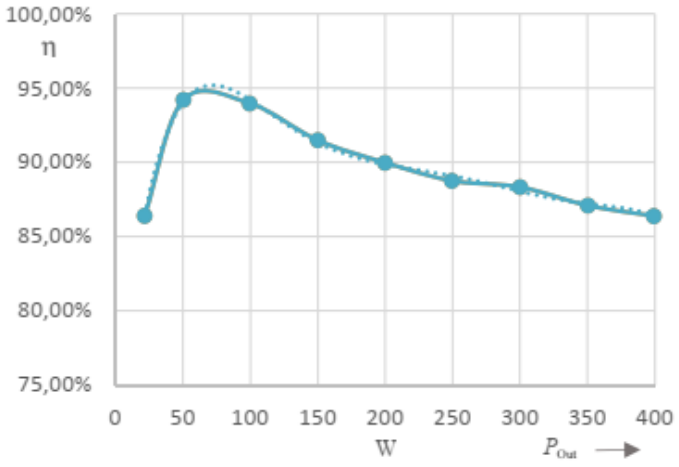

Figure 2.33 Efficiency dependency on output power.

These efficiency levels are comparable to those of a traditional buck converter. However, the hybrid buck L converter offers significant advantages, particularly when handling large voltage differences.

Conclusion

Buck converters are widely used in various applications for electrical power supply, with the filter circuit significantly contributing to the overall volume, weight, and cost. Therefore, accurately determining the required filter size is essential to avoid oversizing.

This papers, [8] - [9] and [1] analyses the hybrid buck *L* converter, which is particularly suitable for applications with wide voltage conversion ratios. A notable disadvantage of this converter is the complexity of the filter elements. However, by using multiphase structures and interleaved switching techniques, the filter requirements can be reduced. Current calculations for a hybrid buck *L* DC-DC converter with varying numbers of phases were performed and compared with simulations and practical measurements of a realized two-phase converter. The results show that the input and output capacitor currents are significantly reduced, [8] - [9] and [1].

In multiphase configurations, phase current balancing is necessary, requiring common mode inductors at each phase output. These inductors must fully compensate for any imbalance, adding complexity to the circuit design and increasing the circuit's overall effort.

Finally, the efficiency results of the realized converter are presented. The converter has a nominal output power of 400W with an input voltage of 50V, demonstrating high efficiency in operation [8] - [9] and [1].

2.1.1.2 Multiphase Buck-Boost-L converter

In the paper, [13], a novel structure of a DC-DC multiphase converter is presented, specifically a buck-boost topology. Although this converter was initially proposed in the PhD thesis, [1], the detailed analysis of the buck-boost multiphase converter variant has not been published then. Like in the previous work, this paper, [13], follows a systematic approach, beginning with the abstract and introduction, followed by an analysis of the single-phase converter.

The discussion, then progresses to the two-phase and a *n*-phase interleaved design can be read also from the article. Simulations, along with practical measurements, validate the theoretical analysis, confirming the effectiveness of the multiphase configuration.

The structure of the converter for a two-phase and an *n*-phase interleaved hybrid buck-boost *L*-converter can be seen in the Figure 2.34

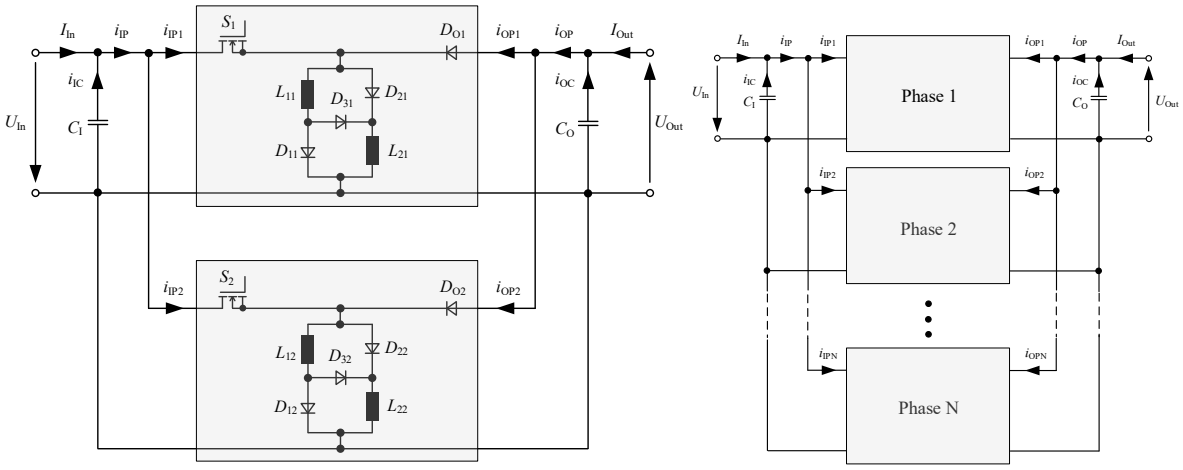

Figure 2.34 Design of a two-phase (left) and an *n*-phase (right) interleaved hybrid buck-boost *L* converter.

The conversion ratio of the hybrid buck-boost converter is:

$$U_{\mathrm{Out}} = \frac{2 \cdot d}{1-d} \cdot U_{\mathrm{In}} \qquad (2.16)$$

with $d = \frac{t_{\mathrm{on}}}{T_P}$ and $1 - d = \frac{t_{\mathrm{off}}}{T_P}$.

The currents for the two-phase hybrid buck-boost converter presented in Figure 2.34, are shown in Figure 2.35. The figure's top section, highlighted in yellow, displays the currents in both inductors and the input current for phase 1, while the bottom section, in green, illustrates the corresponding currents for phase 2. The triangular inductor currents of the two phases are shifted by half a pulse period. During the *on*-state, the inductors for each phase are connected in parallel, resulting in an input current for each phase that is double the inductor current, with the phase output currents at zero. In the *off*-state, the inductors connect in series, making the phase output currents equal to the inductor currents, while the phase input currents are zero, [13].

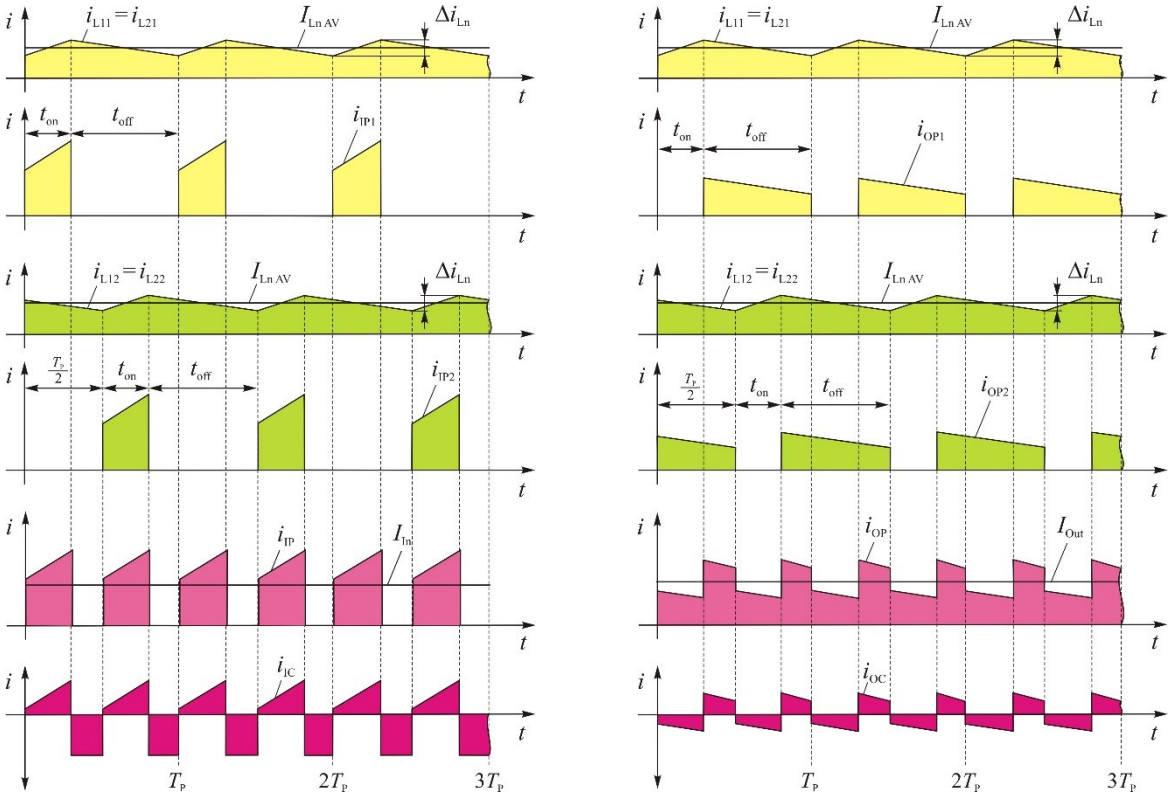

Figure 2.35 Current waveforms at the input (left) and output (right) of a two-phase buck-boost converter.

The overall input phase current, I_{IP}, is the sum of the input phase currents, while the total output phase current, I_{OP}, is the combined current from the output phases. In the Figure 2.35, the overall input phase current I_{IP} with its *DC* component I_{In} is shown on the left, and the overall output phase current I_{OP} with its *DC* component I_{Out} appears on the right. For this circuit, it is assumed that only *DC* currents flow through the input and output. Under these conditions, the relationship between the input current I_{In}, output current I_{Out}, and the average inductor current of each phase I_{LnAV} for multiphase converters can be determined.

$$I_{\mathrm{Ln\,AV}} = \frac{\mathrm{I_{In}}}{\mathrm{n}\cdot(2\cdot\mathrm{d})} \quad (2.17)$$

$$I_{\mathrm{Ln\,AV}} = \frac{I_{\mathrm{Out}}}{n\cdot(1-d)} \quad (2.18)$$

The *AC* component of the overall input phase current, I_{IP}, flows into the input capacitor, while the *AC* component of the overall output phase current, I_{OP}, flows through the output capacitor. These capacitor currents are significantly smaller compared to those in a single-phase hybrid buck-boost converter, and the frequency of these currents is doubled, allowing for reduced filtering requirements, [13].
The RMS currents in the input and output capacitors are calculated. In Figure 2.36, the RMS currents for single-, two-, and three-phase buck-boost converters are shown. The input capacitor current is roughly twice that of the output capacitor, and the RMS current load on both capacitors decreases as the number of phases increases. These currents can be divided into two components: a rectangular part and a triangular part. The rectangular RMS component is dominant (shown with dotted lines when $\Delta i_{\mathrm{Ln\,max}} = 0$), and its maximum contribution to the capacitor current decreases by a factor of $1/n$ for an n-phase converter.
Calculations show that the triangular component has minimal influence on the total current in the capacitors of multiphase converters. Therefore, the triangular current in the inductors can be increased, improving the dynamic response of the hybrid buck-boost DC-DC converter while significantly reducing the inductance and capacitance requirements, [13].

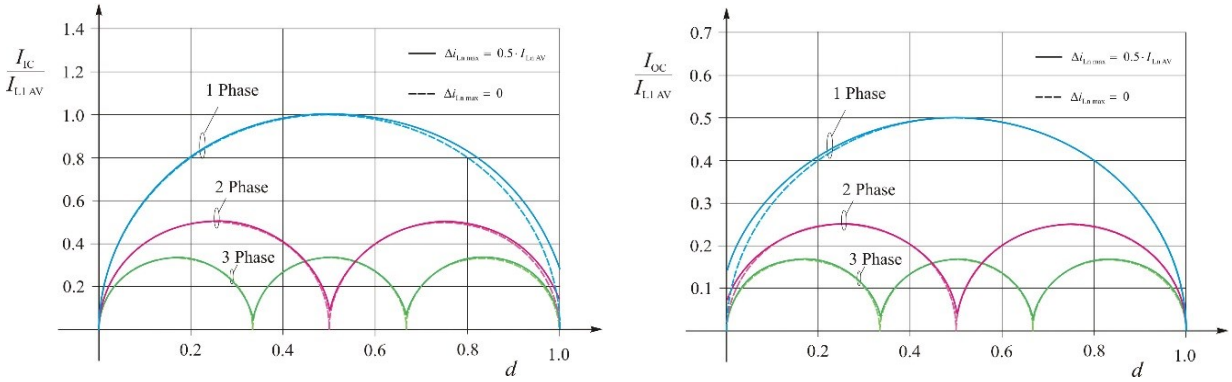

Figure 2.36 RMS-Current in input (left) and output capacitors (right) of converters with different phases.

In addition to the calculated current in the capacitors, harmonics generated by the switching processes in each phase also flow through the capacitors. Studies published in [9], [48] and [51], examined this additional current in a different converter, and these findings are applicable also to this hybrid buck-boost converter. At low loads, this extra current can significantly impact the capacitors and increasing their temperature. However, as output power rises, the calculated capacitor current becomes more dominant. The impact of this additional current is influenced by the converter's pulse frequency. In the paper, [13], can be seen also the results from the practical part. In this habilitation thesis, will be presented the resume from practical part.

Practical measurements of two-phase hybrid Buck-Boost converter

The circuit is designed for an output power of P_{Out} = 300W. A 600V MOSFET switch and output diode are chosen for each phase, allowing for a wide input and output voltage range. The

hybrid buck-boost converter operates at a pulse frequency of $f_P = 25$ kHz, resulting in a 50 kHz load on the input and output capacitors, [13].

The next figure illustrates the converter's power section (left) with four individual boards and the control board (right). The top two power boards represent one phase, while the bottom two represent the other phase of the hybrid buck-boost converter. The input and output circuits of the converter with the MOSFET and the output diode are placed on the left-hand boards for both phases. In order to control the MOSFETs, a gate driver circuit is mounted on these boards. Each of the two power boards on the right contains the circuit structure for each phase, including two inductors and three diodes. The inductors in each phase are magnetically coupled. Additionally, current sensors are used to measure the current in both inductors as well as at the phase input and output for each phase, [13].

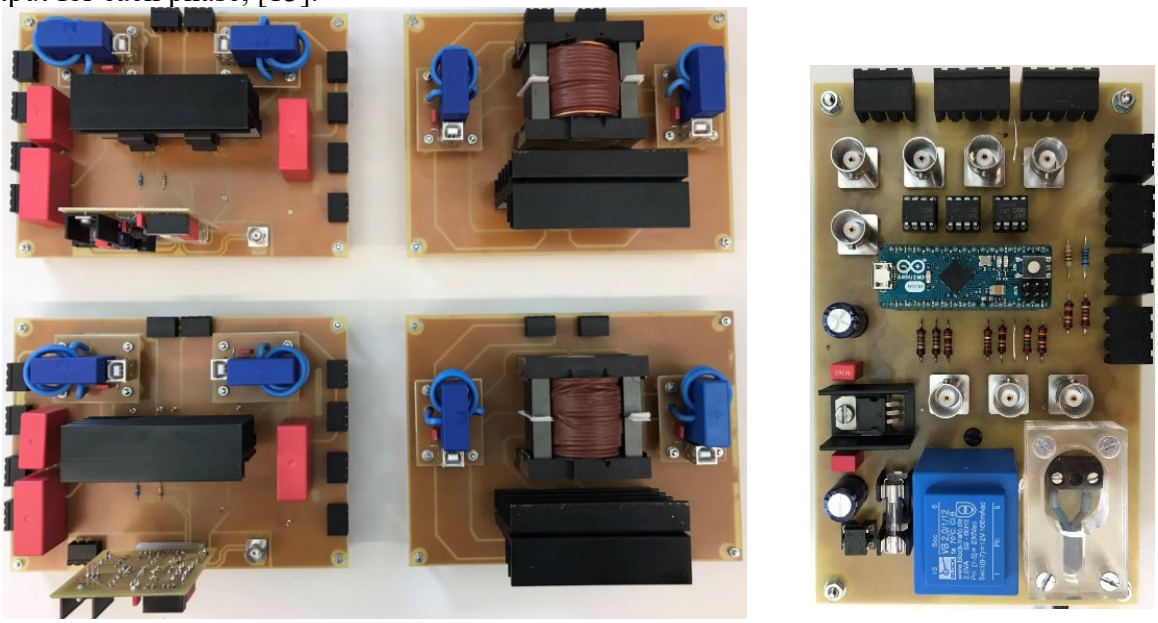

Figure 2.37 Photos of the two-phase buck-boost converter power (left) and control board (right).

In Figure 2.38, waveforms of the hybrid buck-boost converter are shown for a duty cycle of $d = 0.33$ (left) and $d = 0.5$ (right). The current scale is set to 3.33 A/div, and the time scale to 10 µs/div, with zero lines marked on the left of each diagram. The upper section of the figure displays the nearly constant, triangular inductor currents alongside the phase input currents from the two-phase converter. During the *on*-state, the phase input current is twice the inductor current. In the *off*-state, the inductor currents flow through the output diode to the phase output, as shown in the lower part of the figure.

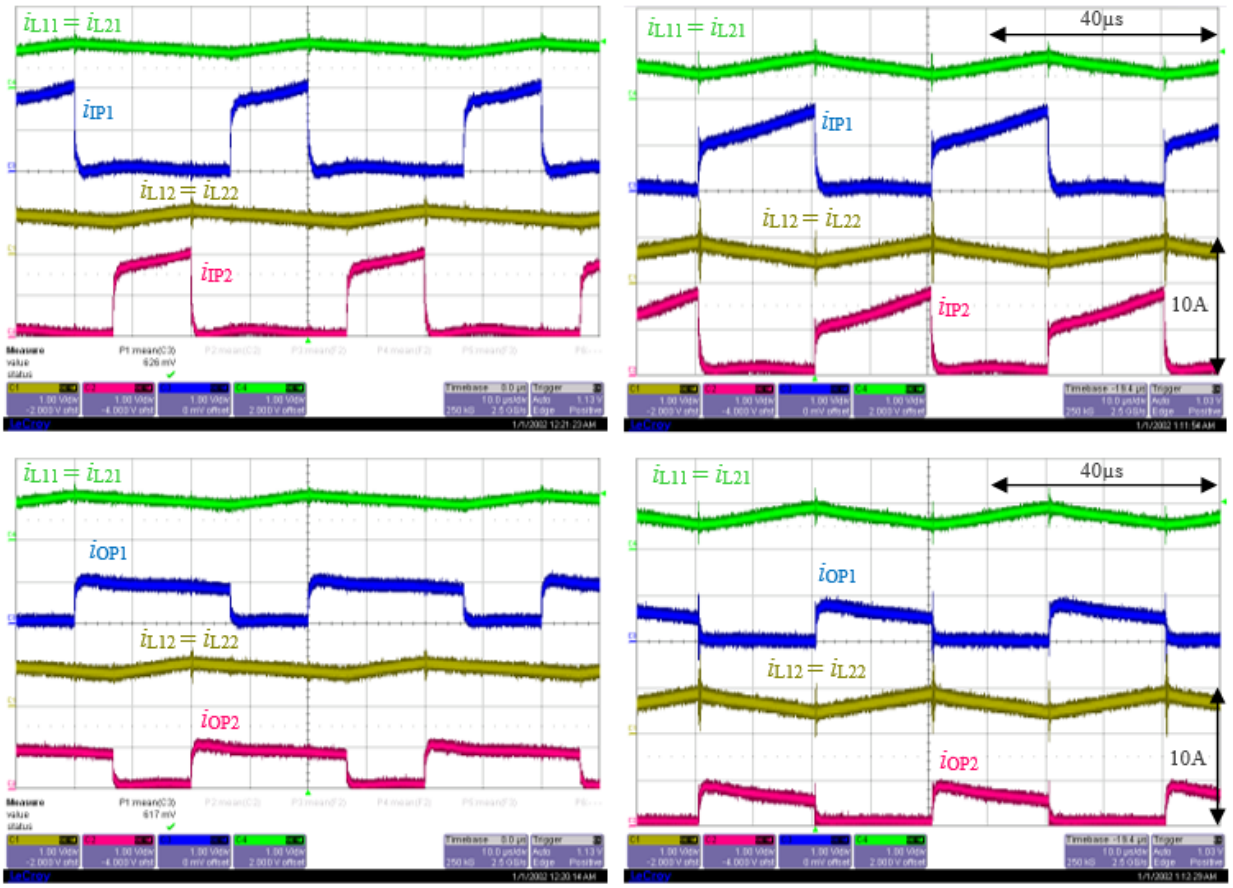

Figure 2.38 Current waveforms of the converter at a duty cycle $d = 0.33$ (left) and $d = 0.5$ (right).

In Figure 2.39, efficiency diagrams for the implemented two-phase hybrid buck-boost converter are shown. The input voltage, $V_{In} = 60V$, remains constant, while the output voltage varies in 30V increments from $V_{Out} = 60V$ to $V_{Out} = 150V$. The typical efficiency curve for $V_{Out} = 60V$ is displayed in the top left, with a peak efficiency of 91.5% and a decrease to 89% at full load. At $V_{Out} = 90V$, efficiency improves slightly, reaching 91.5% at rated power. For $V_{Out} = 120V$, efficiency further increases, achieving 92.5% at rated power. With $V_{Out} = 150V$, efficiency rises again, reaching around 93%, maintaining nearly constant performance over a wide power range, [13].

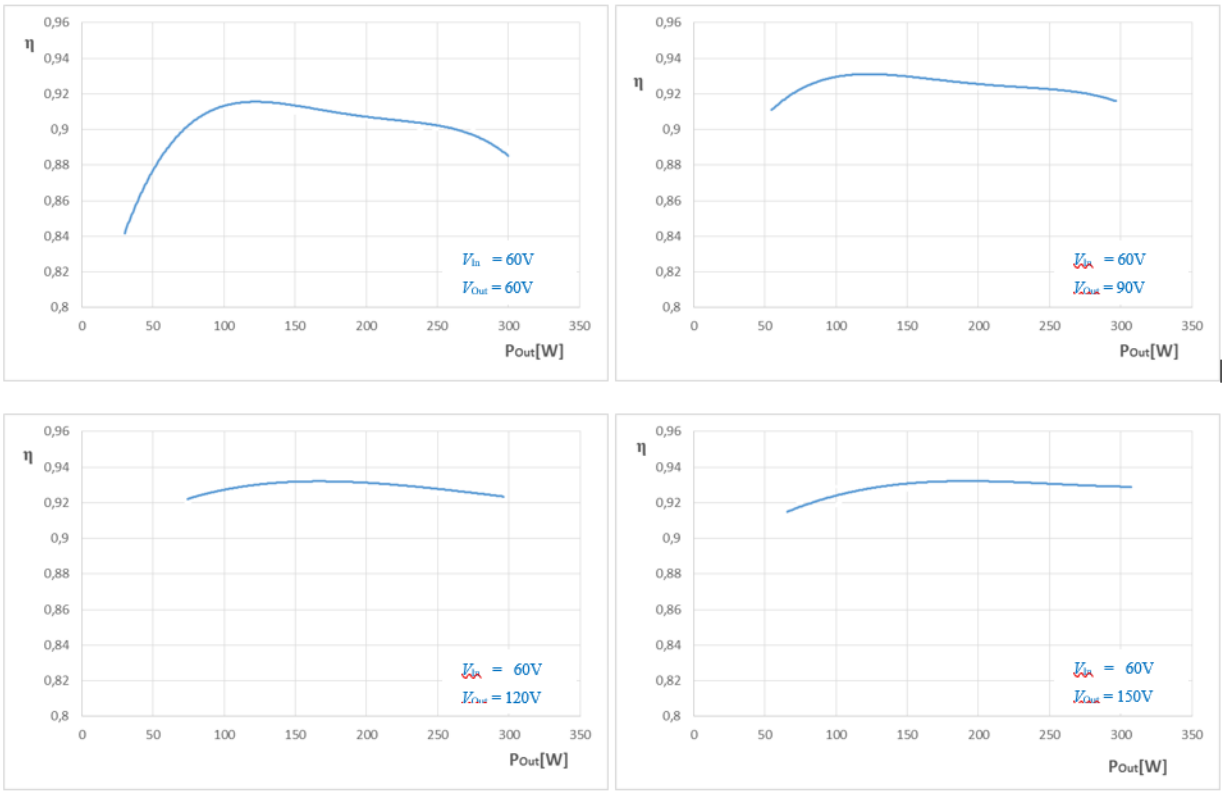

Figure 2.39 Efficiency diagrams for the two-phase hybrid buck-boost converter.

In the conclusion's sections of the paper, are presented the main features of this converter and it is followed by a comprehensive list of references.

2.1.1.3 Hybrid Boost-L converter

The paper "A New Hybrid Boost-*L* Converter", [11], introduces a new step-up topology with a high step-up conversion ratio, [11]. In comparison to a classical boost converter, [2], the static conversion ratio is $(1+n \cdot D)$ times higher, where n is the transformer ratio. Unlike quadratic converters, this design uses only one transistor, three diodes, one capacitor, and one magnetic component, effectively reducing the reactive elements. Design equations are provided, with simulations and experimental results validating the theoretical performance. This novel converter presents a cost-effective solution for applications requiring a substantially higher output voltage than the input voltage [11].

The development of this converter started from the hybrid step-up converter with switching structure Up3 [7], as shown in Figure 2.40 and analysed in [7], [52], [47]. The initial step in developing the new structure was to couple the two inductors and to analyse the converter operation. For transformer ratios *higher* than unity, diode D_4 remains always *off* and therefore it was eliminated, simplifying the circuit and reducing the costs. Additionally, coupling the inductors reduces the need for an additional magnetic core, simplifying the design even more. The resulting

converter, shown in Figure 2.41, includes one active switch, three passive switches, an output capacitor, and two coupled inductors, achieving a distinct conversion ratio.

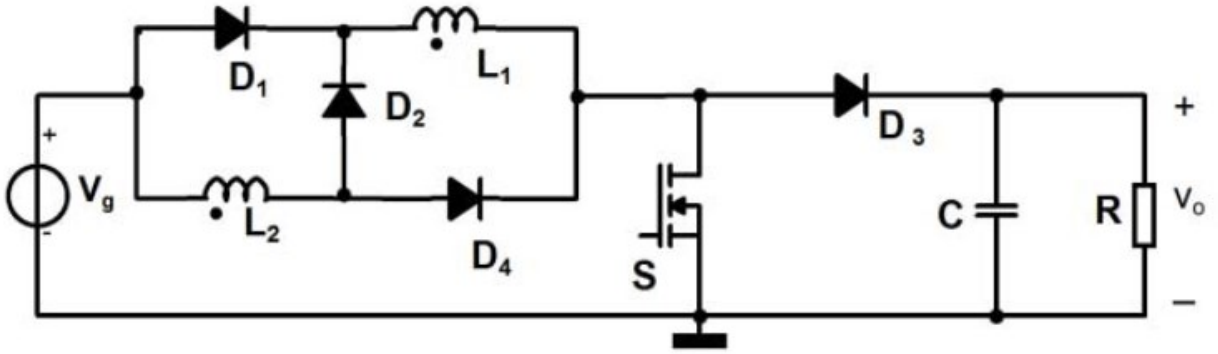

Figure 2.40 Hybrid step-up converter with switching structure Up3 [7].

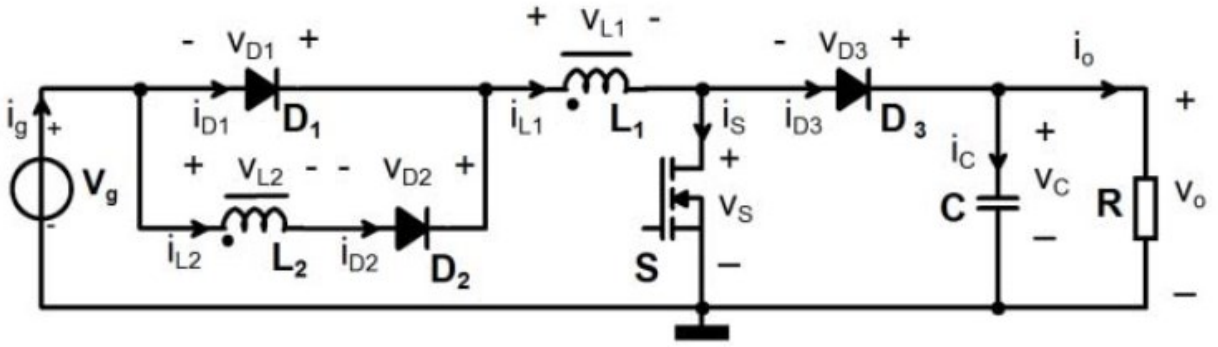

Figure 2.41 The new proposed Hybrid Boost-*L* converter [11].

The *DC* analysis is conducted for continuous conduction mode (*CCM)*, focusing on diodes D_1, D_2, and D_3. Typical for *CCM* analysis, small ripple assumptions are made for the state variables, considering inductor currents and capacitor voltages nearly constant for *DC* analysis purposes, and the static conversion ratio is derived under these conditions. Ideal operation is assumed, where all components are lossless, and the inductors are perfectly coupled.
For this hybrid Boost-*L* converter operating in *CCM*, two topological states are possible, based on the switching states of the power transistor and diodes. The switching frequency is denoted by f_s and the period by T_s, with the transistor duty cycle represented by D. During the first state, from 0 to $D \cdot T_s$, transistor S and diode D_1 are on, while diodes D_2 and D_3 are off due to reverse biasing.
In the second state, from $D \cdot T_s$ to T_s, transistor S and diode D_1 turn off, and diodes D_2 and D_3 are forward biased. To facilitate the analysis, an equivalent schematic is used as in Figure 2.42, where the coupled inductors are replaced by an ideal transformer (denoted *IT*) and a magnetizing inductance L_M, equal to L_1, with the transformer ratio denoted as n.

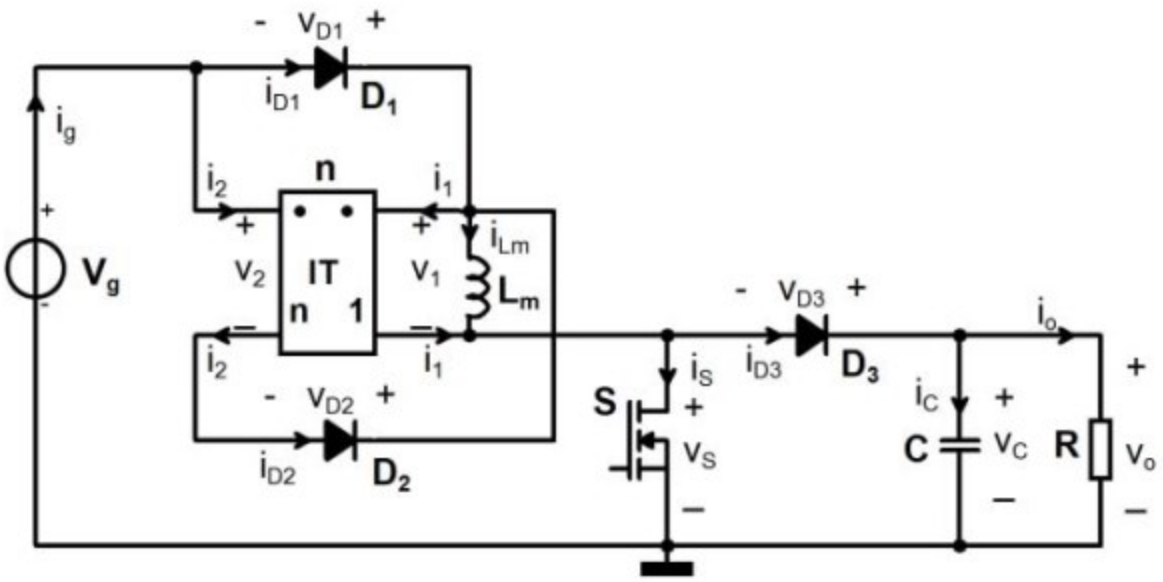

Figure 2.42 Equivalent schematic of the proposed Hybrid Boost-*L* converter.

The ideal transformer equations are:

$$i_1 + n \cdot i_2 = 0 \qquad (2.19)$$

$$v_2 = n \cdot v_1 \qquad (2.20)$$

and these equations are applied to any converter configuration that incorporates coupled inductors. The *DC* voltage across the output capacitor is equal to output voltage and is:

$$V_C = V_o = \frac{1+n \cdot D}{1-D} \cdot V_g \qquad (2.21)$$

Hence the static conversion ratio of the converter is:

$$M = \frac{1+n \cdot D}{1-D} \qquad (2.22)$$

The dependency of the static conversion ratio against duty cycle, with $n>1$ as a parameter, is presented in Figure 2.43.

The dc value of the magnetizing current is:

$$I_{LM} = \frac{(n+1) \cdot (1+n \cdot D)}{(1-D)^2} \cdot \frac{V_g}{R} \qquad (2.23)$$

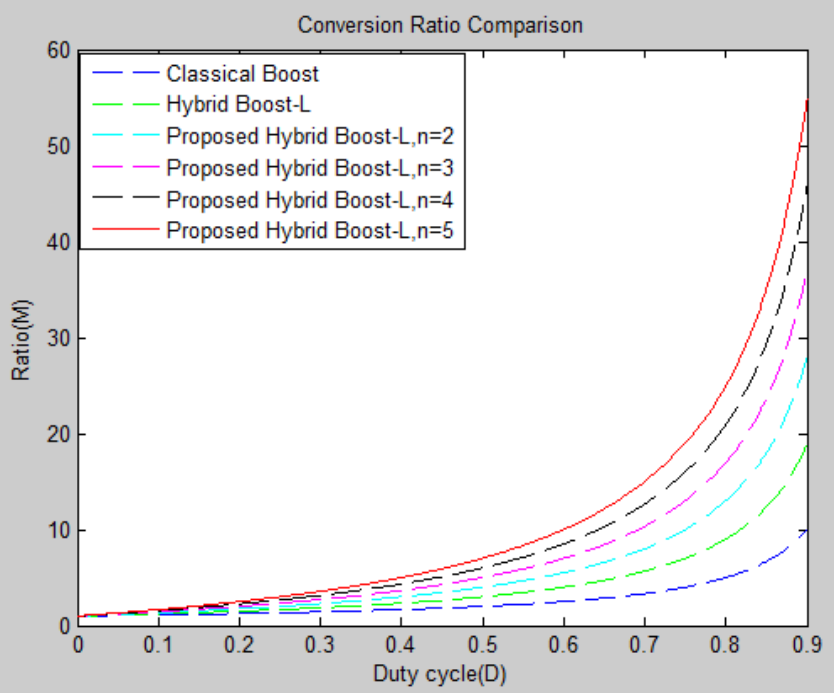

Figure 2.43 Static conversion ratio against duty cycle for the proposed converter (where *n*=2-5), classical Boost converter and Hybrid Boost-*L* converter from [7].

The semiconductors current and voltage stresses are presented in Table 2.1.

Table 2.1 Device stresses.

Name of the component	Voltage	Current
S	$V_S = \frac{1+n\cdot D}{1-D}\cdot V_g$	$I_S = \frac{(n+1)\cdot(1+n\cdot D)\cdot D}{(1-D)^2}\cdot\frac{V_g}{R}$
D_1	$V_{D1} = \frac{n\cdot D}{1-D}\cdot V_g$	$I_{D1} = \frac{(n+1)\cdot(1+n\cdot D)\cdot D}{(1-D)^2}\cdot\frac{V_g}{R}$
D_2	$V_{D2} = n\cdot V_g$	$I_{D2} = \frac{(1+n\cdot D)}{1-D}\cdot\frac{V_g}{R}$
D_3	$V_{D3} = \frac{1+n\cdot D}{1-D}\cdot V_g$	$I_{D3} = \frac{1+n\cdot D}{1-D}\cdot\frac{V_g}{R}$

Different step-up converters supplied from the same input voltage, V_g, while providing the same output voltage, V_o, to the same load, R, are taken into consideration for a fair comparison. The results of this comparative analysis are presented in Table 2.2, [11].

Table 2.2 Comparison between main parameters of different step-up converters.

Parameter	Type of Boost Converter			
	Classic	Hybrid Up1	Hybrid Up3	Proposed
Switches	1	1	1	1
Diodes	1	2	4	3
Total no. of components	4	8	8	7
System Order	2	3	3	3
Conversion ratio - M	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1+n\cdot D}{1-D}$
Switch voltage stress	$M\cdot V_g$	V_g	$M\cdot V_g$	$M\cdot V_g$
Switch current stress	$M\cdot\frac{V_g}{R}$	$M\cdot\frac{V_g}{R}$	$M\cdot\frac{V_g}{R}$	$M(M-1)V_g/R$
Diode voltage stress	$M\cdot V_g$	$\frac{(1-M)\cdot V_g}{2}$	$M\cdot V_g$	$M\cdot V_g$
Diode current stress	$M\cdot\frac{V_g}{R}$	$M\cdot\frac{V_g}{R}$	$M\cdot\frac{V_g}{R}$	$M\cdot\frac{V_g}{R}$
Input current	Smooth	Smooth	Smooth	Smooth

It can be remarked that the static conversion ratio is higher than that of classical Boost converter, even higher than that of the hybrid Boost *L* converter from [7]. The converter uses a lower number of diodes, than the Hybrid Up 3 and less components than the Hybrid Up1 and Hybrid Up3. All converters exhibit smooth input current. This feature makes the new converter highly suitable for applications requiring high output voltages.
To design the proposed boost converter, the following specifications are considered, Table 2.3.

Table 2.3 Design specifications.

Parameter name	**Value**
Input voltage Vg	30V
Output voltage V_o	120V
Output power P_o	50W
Switching frequency f_s	50 kHz
Transformer ratio n	2

Knowing the design specifications, the values of the components were calculated. The resulted static conversion ratio is $M=V_o/V_g=4$, the duty cycle $D=\frac{M-1}{M+n}=0.5$ and the load resistor $R=V_o^2/P_o=288\Omega$. From the calculations $L_M=L_1=122.10$ µH and $L_2=n^2\cdot L_M=488.40$ µH were obtained. The value of the minimum capacitor was $C_{min}=3.472$ µF but was chosen the standard value of 4.7 µF. In the next figures the results of simulation can be seen. Because of the coupled

inductors, only half of the triangular shape of the magnetizing current will be seen through the first inductor, Figure 2.46, and the other half triangular shape through the second inductor, Figure 2.48.

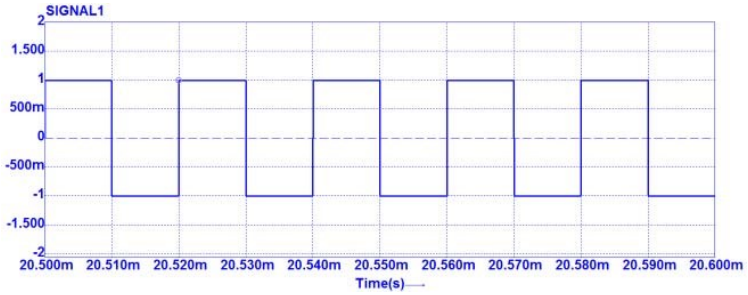

Figure 2.44 PWM signal applied to the gate of the transistor.

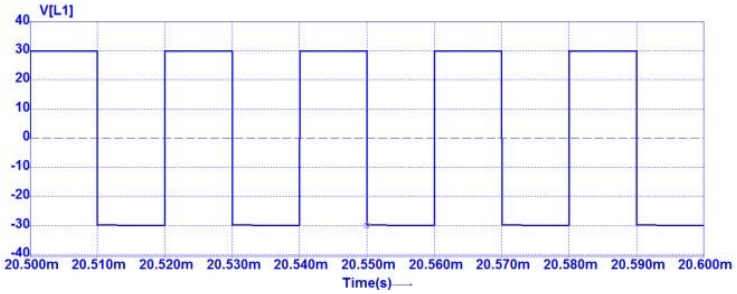

Figure 2.45 Voltage across L_1 coil.

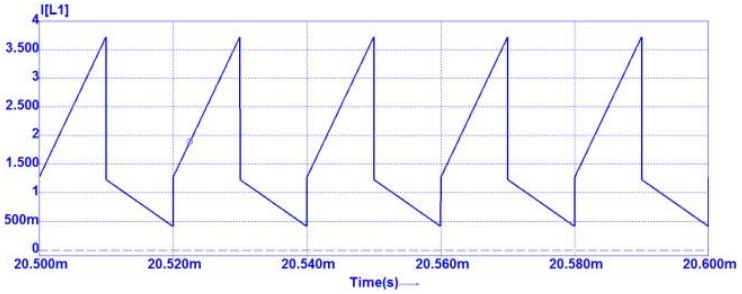

Figure 2.46 Current through inductor L_1.

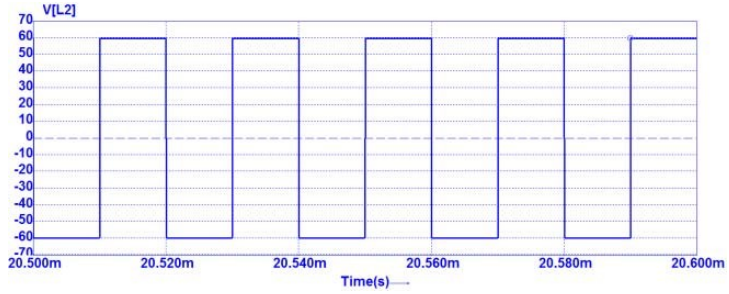

Figure 2.47 Voltage across L_2 coil.

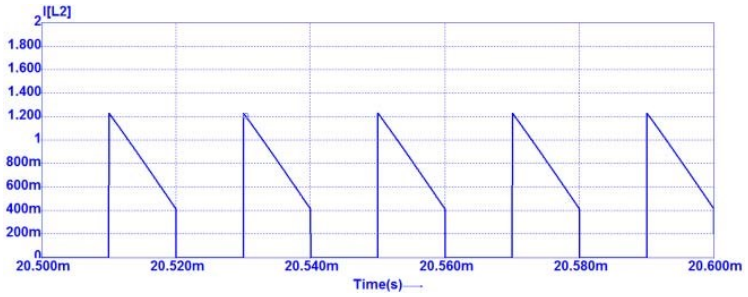

Figure 2.48 Current through inductor L_2.

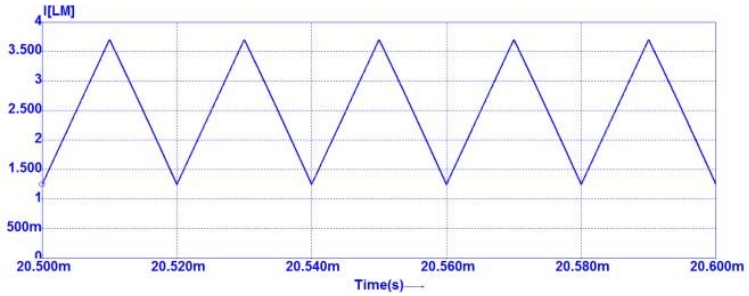

Figure 2.49 Current through the magnetizing inductor L_M.

A practical prototype of the simulated converter was developed to validate its performance against theoretical predictions. Minor differences in component values, along with parasitic elements, introduce slight deviations from the designed values. The setup includes an NXP MOSFET BUK455-200 A as the switch, UF5402 rectifiers for diodes D_1, D_2, and D_3, and inductors L_1=122.10 µH and L_2=523.60 µH. Oscilloscope captures in Figure 2.50 and Figure 2.51 show the waveforms for transistor voltage, output voltage, and currents/voltages across L_1 and L_2, closely agreeing with simulation, [11].

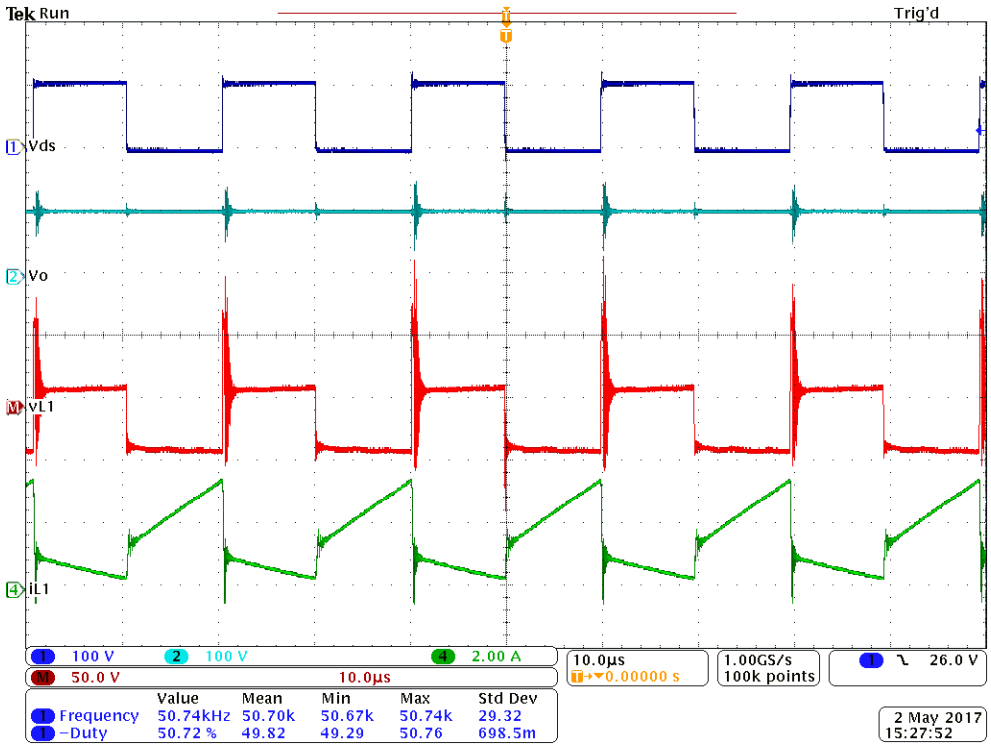

Figure 2.50 Oscilloscope waveforms: voltage across the transistor, drain to source (dark blue – V_{ds}); output voltage light blue-V_o); voltage across L_1 (red- v_{L1}); current through L_1 (green- i_{L1}).

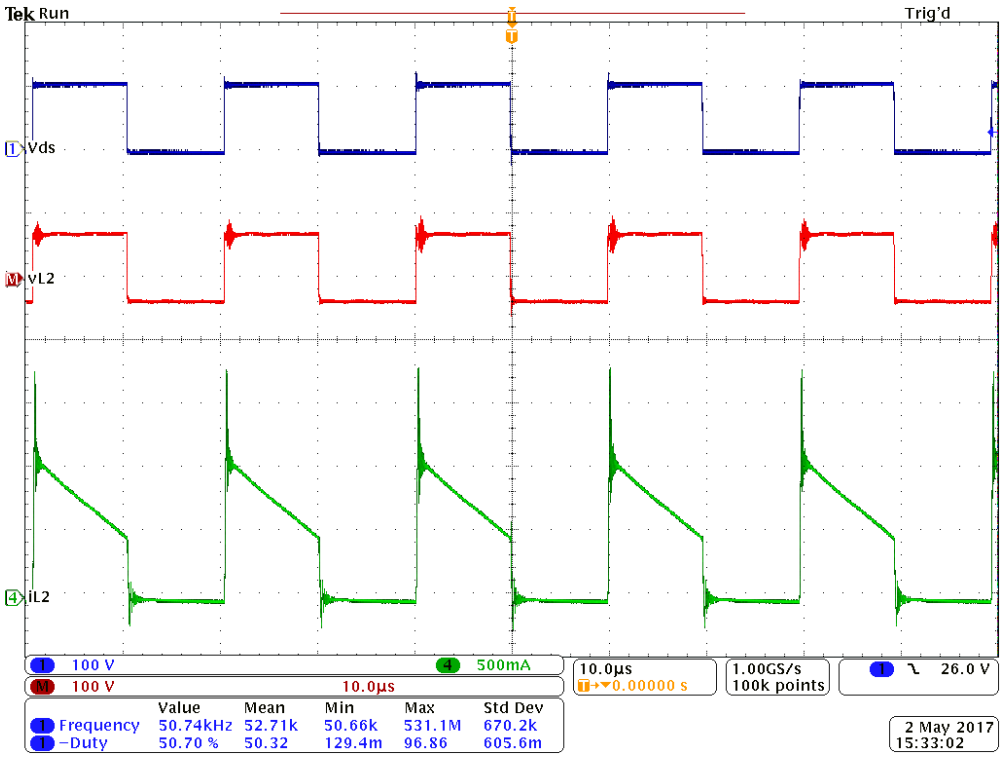

Figure 2.51 Oscilloscope waveforms: voltage across the transistor, drain to source (dark blue – V_{ds}); voltage across L_2 (red- v_{L2}); current through L_2 (green- i_{L2}).

The experimental static conversion ratio was measured and compared to the ideal theoretical curve and the theoretical curve that takes into account the conduction losses, Figure 2.52. The efficiency curve against the duty cycle, from Figure 2.53, shows that experimental results are slightly below theoretical losses characteristic due to additional ripple-induced losses and switching losses.

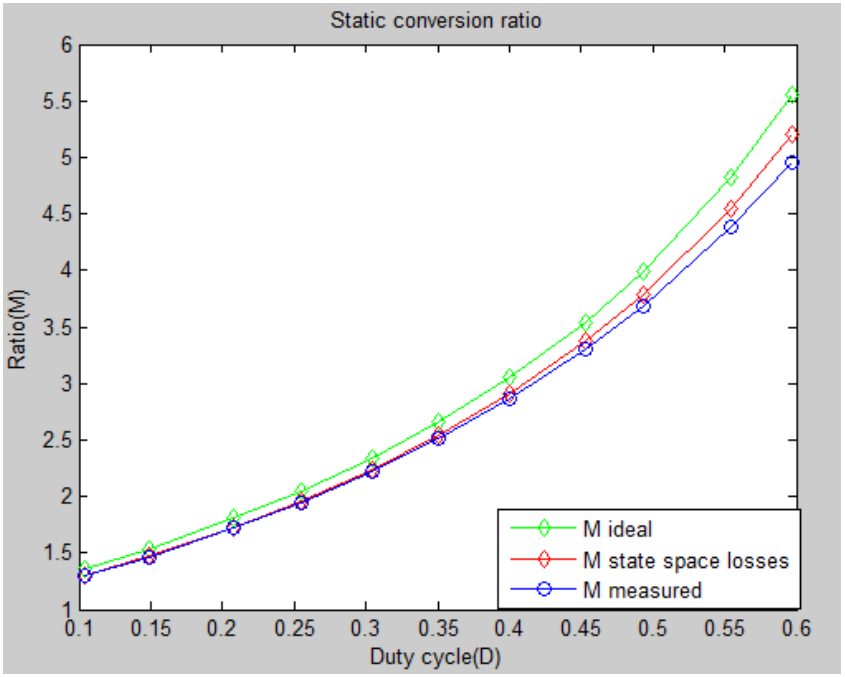

Figure 2.52 The experimental conversion ratio against duty cycle in comparison with the ideal, respectively with losses calculated.

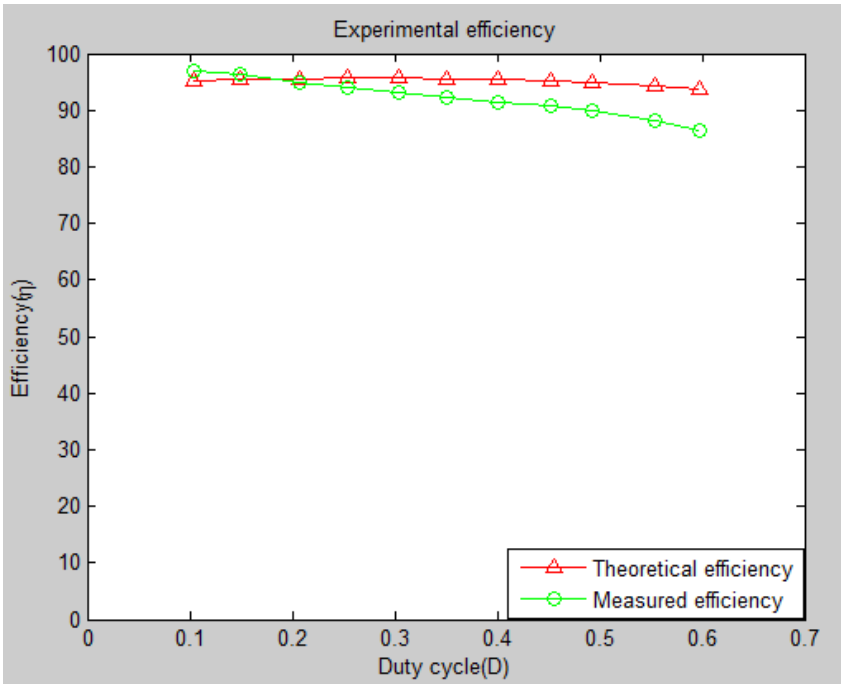

Figure 2.53 The experimental efficiency against the duty cycle.

Overall, these results confirm the feasibility and usefulness of the proposed topology, demonstrating its suitability in step-up high-efficiency applications, [11].

The paper "A Comparison Between Single-Phase and Two-Phase Hybrid Boost-L Converter", [18], compares single-phase [11] and two-phase hybrid Boost-*L* converters, focusing on their design, operation, and performance differences. The single-phase configuration is presented in Figure 2.54, while the two-phase hybrid Boost-*L* converter in Figure 2.55, which employs interleaved switching to achieve better current distribution and reduced filter stress compared to its single-phase counterpart. The two-phase design results in lower RMS currents in capacitors, reducing component stress and enhancing efficiency. The comparison figures of the input and output capacitor currents for single-phase and two-phase configurations, showing the reduced current stress and ripple achieved in the two-phase design are presented in Figure 2.56. Simulation results confirm that the two-phase converter provides more balanced and less ripple output currents, Figure 2.57, highlighting its suitability for high-power applications like PV systems.

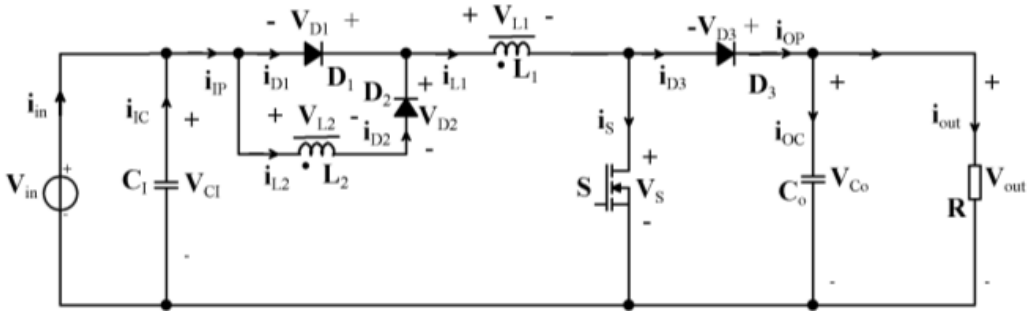

Figure 2.54 Single-phase hybrid Boost- *L* DC-DC converter.

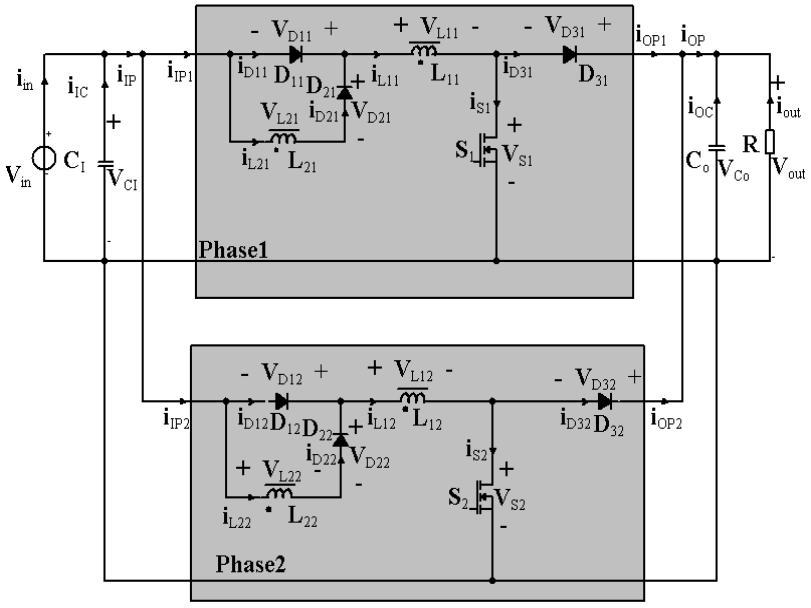

Figure 2.55 Schematic of the interleaved two-phase hybrid Boost- *L* converter.

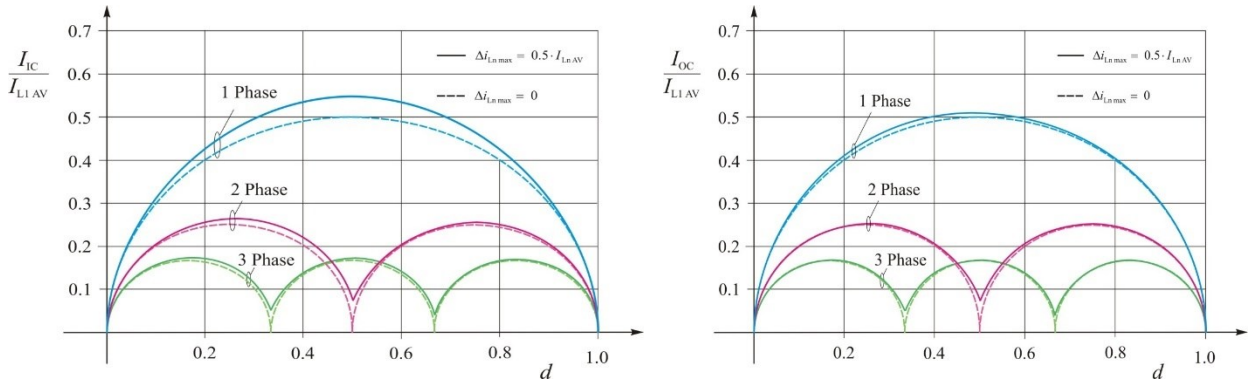

Figure 2.56 RMS input (left) and output (right) capacitor currents for a one-, two- and three-phase converter.

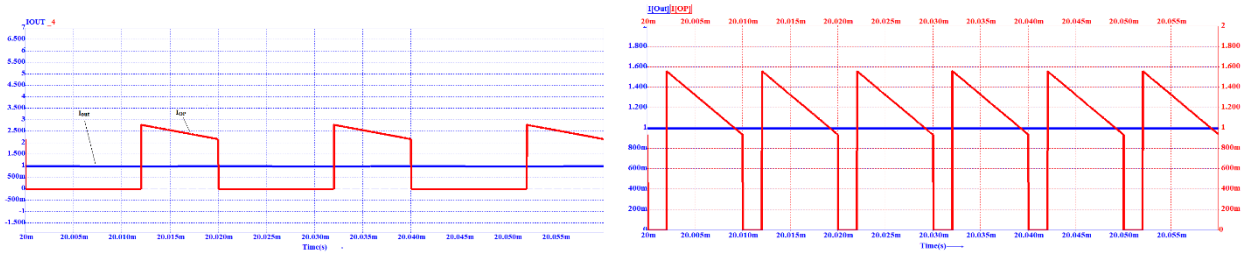

Figure 2.57 Currents at the output of: single-phase converter – left, and two-phase converter – right.

This research that was partial supported by research grants PCD-TC-2017, [42], demonstrates how multiphase configurations can significantly improve DC-DC converter performance because interleaved switching increases the capacitor currents frequency, which significantly reduces the filtering effort as the number of phases increases, [18].

2.1.1.4 Hybrid Buck-L converter with coupled inductors

From the same switching cell family of the Boost-*L* converter presented in Figure 2.41, [11], in [16] is introduced a new Buck-*L* converter obtained using the basic converter cell rotation concept from [53], resulting in the proposed converter shown in Figure 2.58.

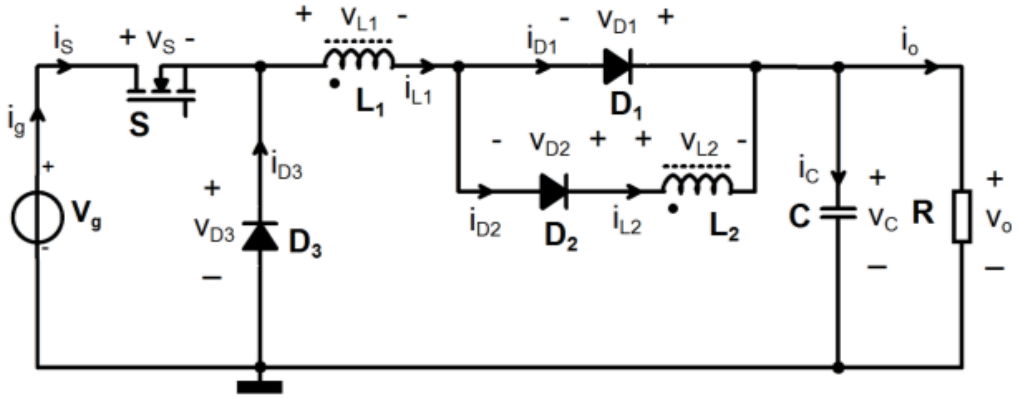

Figure 2.58 The new proposed Hybrid Buck-*L* converter from [16].

Analysing the converter, it results that in CCM, two topological states are defined by the status of the power transistor and diodes. In the first topological state transistor *S* and diode D_1 are on, while diodes D_2 and D_3 are off. In the second topological state transistor *S* and diode D_1 are off, while diodes D_2 and D_3 are on. For the analysis, a simplified schematic is provided in Figure 2.59. The coupled inductors are modelled by an ideal transformer (*IT*) with a transformer ratio *n*, and a magnetizing inductor L_M, which is equal to L_1.

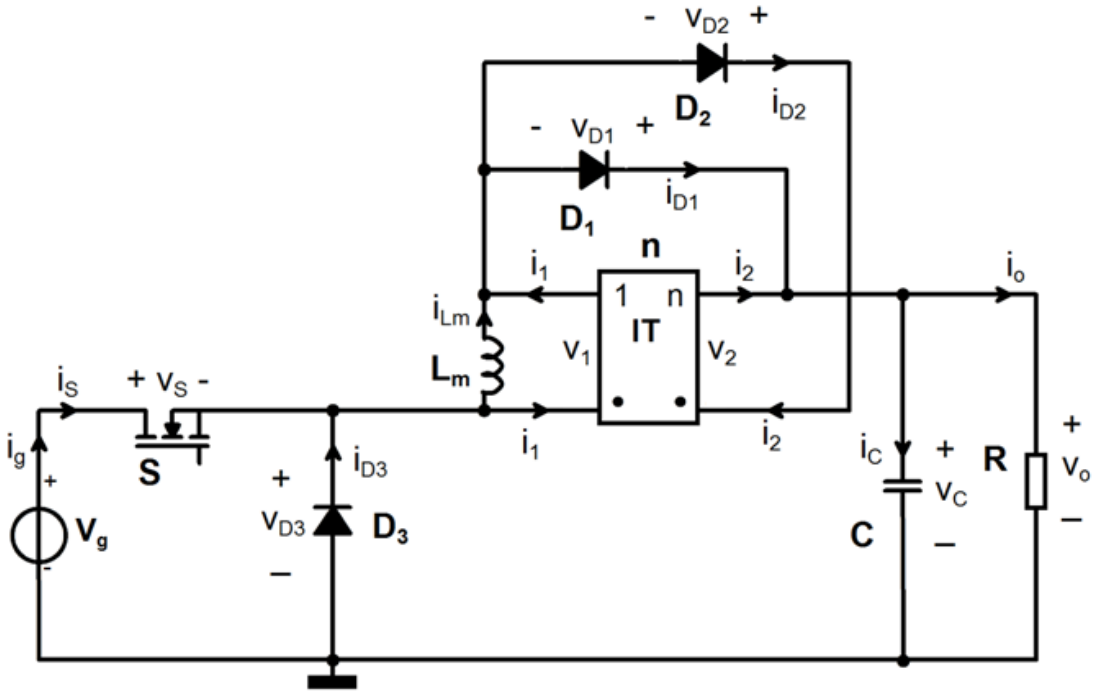

Figure 2.59 Simplified schematic of the proposed Hybrid Buck-*L* converter.

In the paper [16], the operating principles, steady-state analysis, and comparisons with other converters validate its features and the theoretical assumptions. Simulations in the CASPOC program demonstrated excellent agreement with the theoretical considerations. Experimental results further confirmed the simulation and theory, making the converter a reliable choice for practical applications. A short summary of the paper is presented further.

The static conversion ratio of the converter is:

$$M = \frac{(1+n)\cdot D}{1+n\cdot D} \qquad (2.24)$$

The relationship between the conversion ratio and the duty cycle, with $n>1$ as a parameter, is illustrated in Figure 2.60. As shown in Figure 2.60 and derived from equation above, the output voltage is lower than the input voltage, confirming the step-down nature of the converter. For the same duty cycle, the conversion ratio of the proposed converter exceeds that of a traditional Buck converter. Additionally, when the difference between the output voltage V_{out} and the input voltage V_g is small, the proposed converter operates at moderate duty cycles, whereas the classical Buck converter requires unusually high duty cycles.

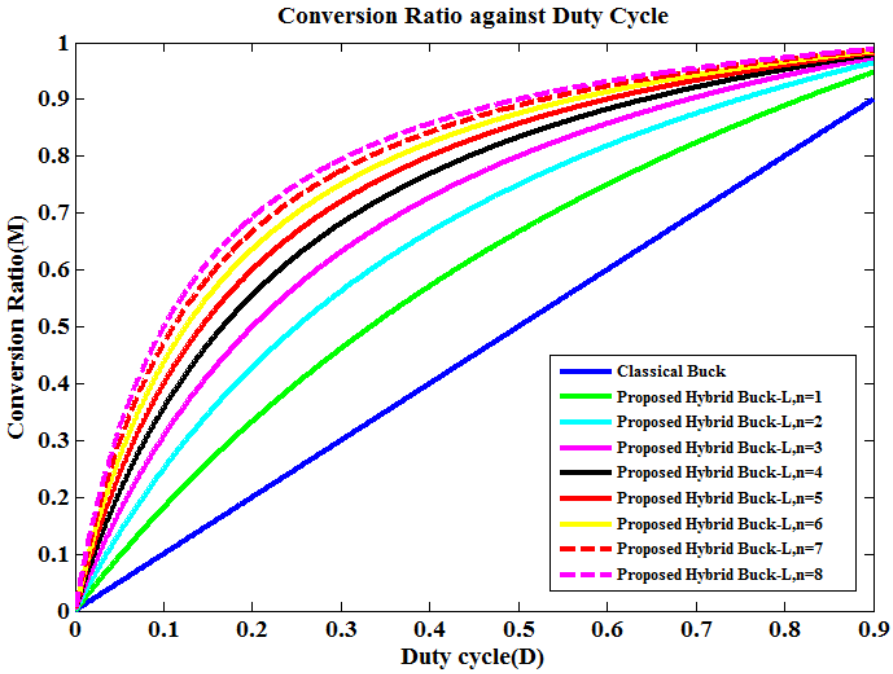

Figure 2.60 Static conversion ratio against the duty cycle for the proposed.

To ensure a fair comparison, various step-down converters are evaluated, all supplied by the identical input voltage V_g and providing the same output voltage V_o at the same load R. Table 2.4 provides a summary of the findings. The novel converter, which has a reasonable number of components, exhibits a switch voltage stress that is comparable to that of the classical, QBC1, QBC3, and QBC4 converters, while diode voltage stress is comparable to that of the classical, QBC2, and hybrid converters. The switch dc current stress is less than that of QBC1 and QBC2, and it is the same to that of the classical, QBC3, QBC4, hybrid, TSQBC, and stacked converters, [16].

Table 2.4 Comparison between main parameters of different step-down converters.

Parameter	Type of Buck Converter								
	Classical	QBC1	QBC2	QBC3	QBC4	Hybrid	TSQBC	Stacked	Proposed
No. of transistors	1	1	1	1	1	1	2	1	1
No. of diodes	1	3	3	3	3	2	3	2	3
Total no. of components	4	8	8	8	8	6	10	8	6
System Order	2	4	4	4	4	3	5	5	2
Conversion ratio (M)	D	D^2	D^2	D (2-D)	D (2-D)	D/(2-D)	D/(2-D)	2D/(1+D)	$\frac{(1+n\cdot)D}{1+n\cdot D}$
Switch voltage stress	V_g	V_g	$(1-\sqrt{M}+2M)\cdot V_g$	V_g	V_g	(1+M)V_g	$\frac{(1+M)}{2}\cdot V_g$	V_g(1-M/2)	V_g
Switch dc current stress	$M^2\cdot\frac{V_g}{R}$	$M\cdot\frac{V_g}{R}$	$M\cdot V_g/R$	$M^2\cdot\frac{V_g}{R}$	$M^2\cdot\frac{V_g}{R}$	$M^2\cdot\frac{V_g}{R}$	$M^2\cdot\frac{V_g}{R}$	$M^2\cdot\frac{V_g}{R}$	$M^2\cdot\frac{V_g}{R}$
Maximum diode voltage stress	V_g	$\sqrt{M}\cdot V_g$	V_g	$\sqrt{1-M}\cdot V_g$	$\sqrt{1-M}\cdot V_g$	V_g	$\frac{(1+M)}{2}\cdot V_g$	V_g(1-M/2)	V_g
Maximum diode current stress	$(1-M)\cdot M\cdot\frac{V_g}{R}$	$M\cdot\frac{V_g}{R}$	$M\cdot\frac{V_g}{R}$	$M\sqrt{1-M}\frac{V_g}{R}$	$M\sqrt{1-M}\frac{V_g}{R}$	$M\cdot\frac{V_g}{2R}$	$M^2\cdot\frac{V_g}{R}$	(1-M)$M\frac{V_g}{R}$	$M^2\cdot\frac{V_g}{R}$

To design the proposed step-down converter, the following specifications are considered, Table 2.5.

Table 2.5 Design specifications.

Parameter name	**Value**
Input voltage V_g	60V
Output voltage V_o	30V
Output power P_o	20W
Switching frequency f_s	50 kHz
Transformer ratio n	1.75

Knowing the design specifications, the components values were calculated. The resulted static conversion ratio is $M=V_o/V_g=0.5$, the duty cycle $D=\frac{M}{1+n-M\cdot n}=0.2666$ and the load resistor $R=V_o^2/P_o=45\Omega$. From the calculations $L_M=L_1=689.23$ µH and $L_2=n^2\cdot L_M=2110.766$ µH were obtained. The practical value used for L_2 was 2113.6 µH. The value of the minimum capacitor was $C_{min}=31.01$ µF, but the standard value of 33 µF was chosen. The transistor voltage stress is $V_S=60$ V, with an average current of $I_S=0.333$ A. The diodes must be selected to handle a reverse voltage of $V_D=60$ V and a DC current of $I_D=0.333$ A. In the next figures the results of the simulations can be seen. Because of the coupled inductors, only half of the triangular shape of the magnetizing current will be seen through the first inductor, Figure 2.61 and the other half triangular shape through the second inductor, Figure 2.62, [16].

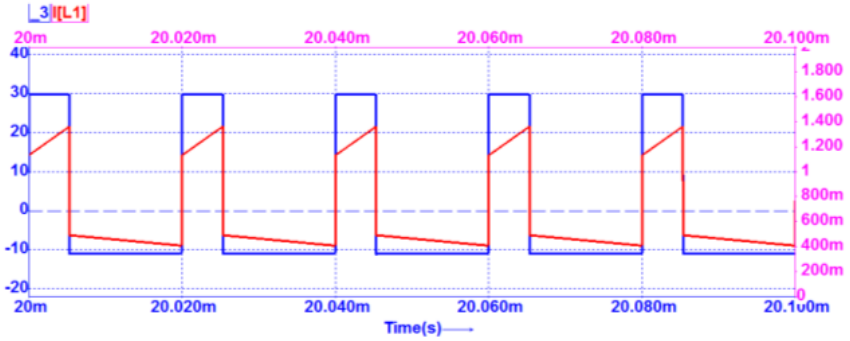

Figure 2.61 Voltage across L_1 (v_{L1} – blue trace) and current through it (i_{L1} – red trace).

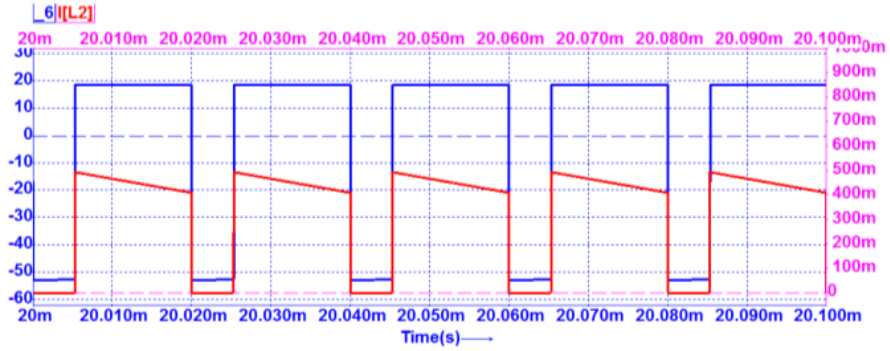

Figure 2.62 Voltage across L_2 (v_{L2} – blue trace) and current through it (i_{L2} – red trace).

A practical experiment was conducted and presented in [16], to validate the theoretical analysis of the proposed converter, using the Infineon Mosfet IPB042N10N3GATMA1 and Vishay Ultrafast rectifiers EGP50F-E3/54. Waveforms from oscilloscope were captured and the voltage across diode D_3 was set as a reference, all showned in Figure 2.63 and Figure 2.64.

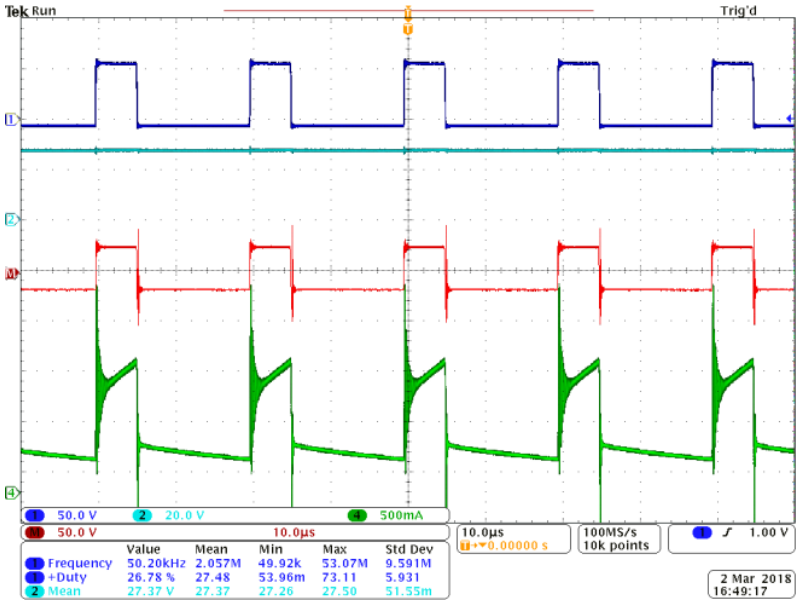

Figure 2.63 Oscilloscope waveforms: voltage across the diode D_3, (dark blue); output voltage (cyan-V_o), voltage across L_1 (red- v_{L1}); current through L_1 (green- i_{L1}).

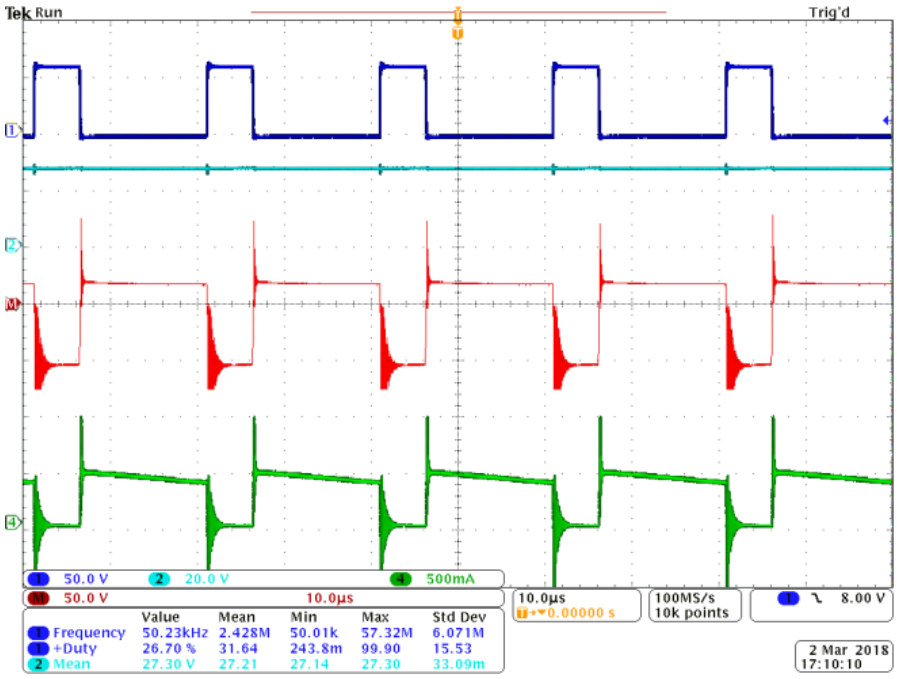

Figure 2.64 Oscilloscope waveforms: voltage across the diode D_3, (dark blue); output voltage (cyan-V_o), voltage across L_2 (red- v_{L2}); current through L_2 (green- i_{L2}).

The experimental static conversion ratios, obtained by varying the duty cycle, showed slightly lower values compared to the theoretical calculations, as illustrated in Figure 2.65, where the experimental curve closely matches the ideal one. Efficiency results, shown in Figure 2.66, demonstrate excellent performance, exceeding 90% for duty cycles $D \geq 0.2$. These results confirm the feasibility and high efficiency of the proposed converter topology.

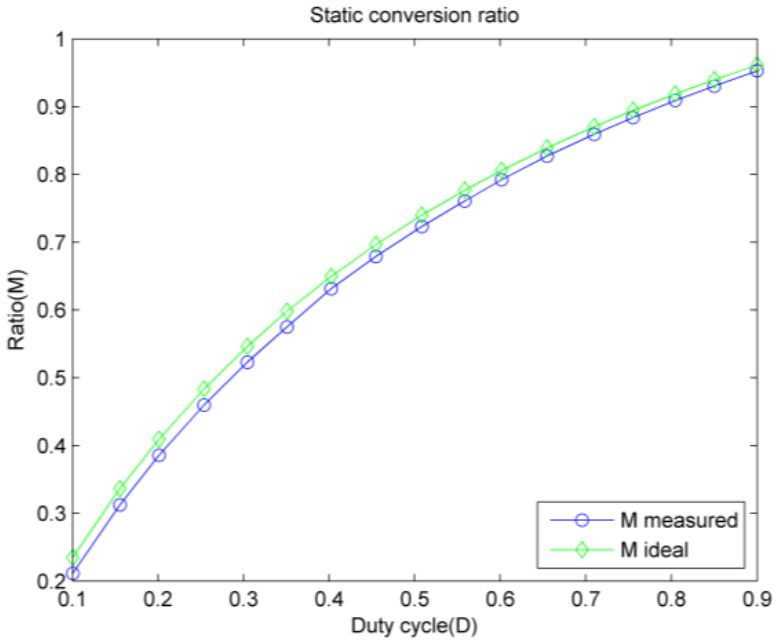

Figure 2.65 The experimental conversion ratio against duty cycle compared to the ideal one.

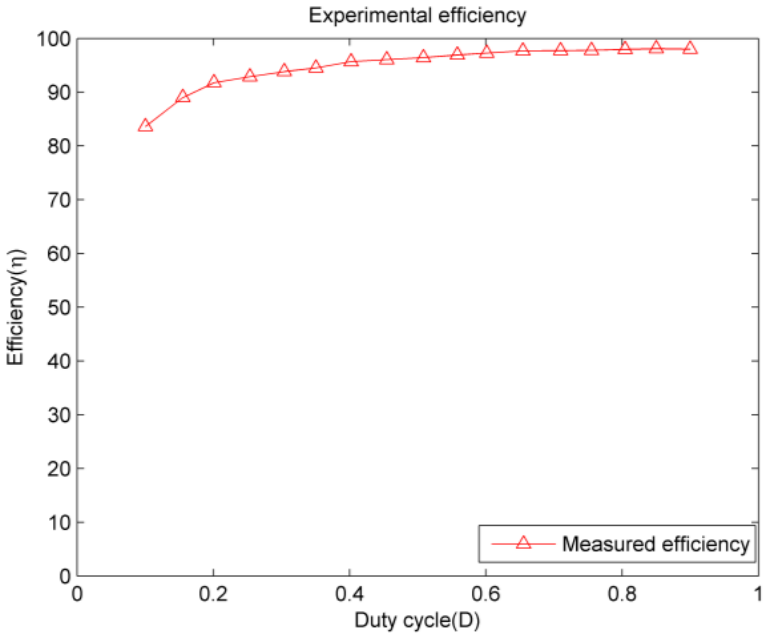

Figure 2.66 The experimental efficiency against the duty cycle.

Conclusion

The proposed hybrid Buck-*L* converter is well-suited for applications requiring an output voltage slightly lower than the input, as it operates efficiently at moderate duty cycles. It features a simple design with one transistor, three diodes, and a magnetic core with two coupled inductors, resulting in a second-order system that simplifies loop design using traditional controllers. This work was supported by a research grant PCD-TC-2017, [42].

2.1.1.5 Hybrid Buck-L converter with unequal inductors

Starting from the Up3 hybrid step-up converter [7], five topologies were synthesized, out of which three are new, including the proposed converter in [32]. The novel step-down topology [32] derived from the hybrid converter [7] is presented in Figure 2.67, consisting of two inductors, an output capacitor, and one transistor. The analysis assumes unequal inductors, showing that the static conversion ratio remains unaffected. The operation involves three states determined by the transistor and diodes conduction, with inductor values influencing diodes behaviour. In the peculiar case when L_1=L_2, the operation involves only two topological states. The simulations and the experiments validated the theoretical analysis, with the key waveforms depicted in Figure 2.68-Figure 2.71.

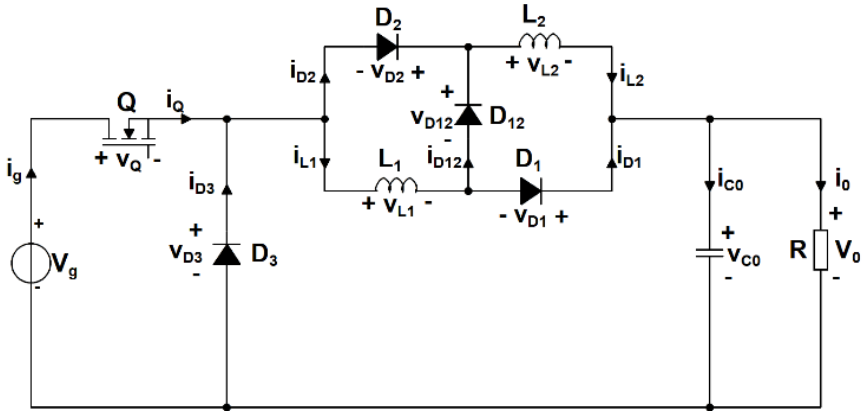

Figure 2.67 The new proposed hybrid Buck-*L* converter.

Converter analyses is a little bit difficult. Even to find out the static conversion ratio, a system with 11 unknowns was solved in Matlab™ [54]. The result is:

$$M = \frac{2D}{1+D} \qquad (2.25)$$

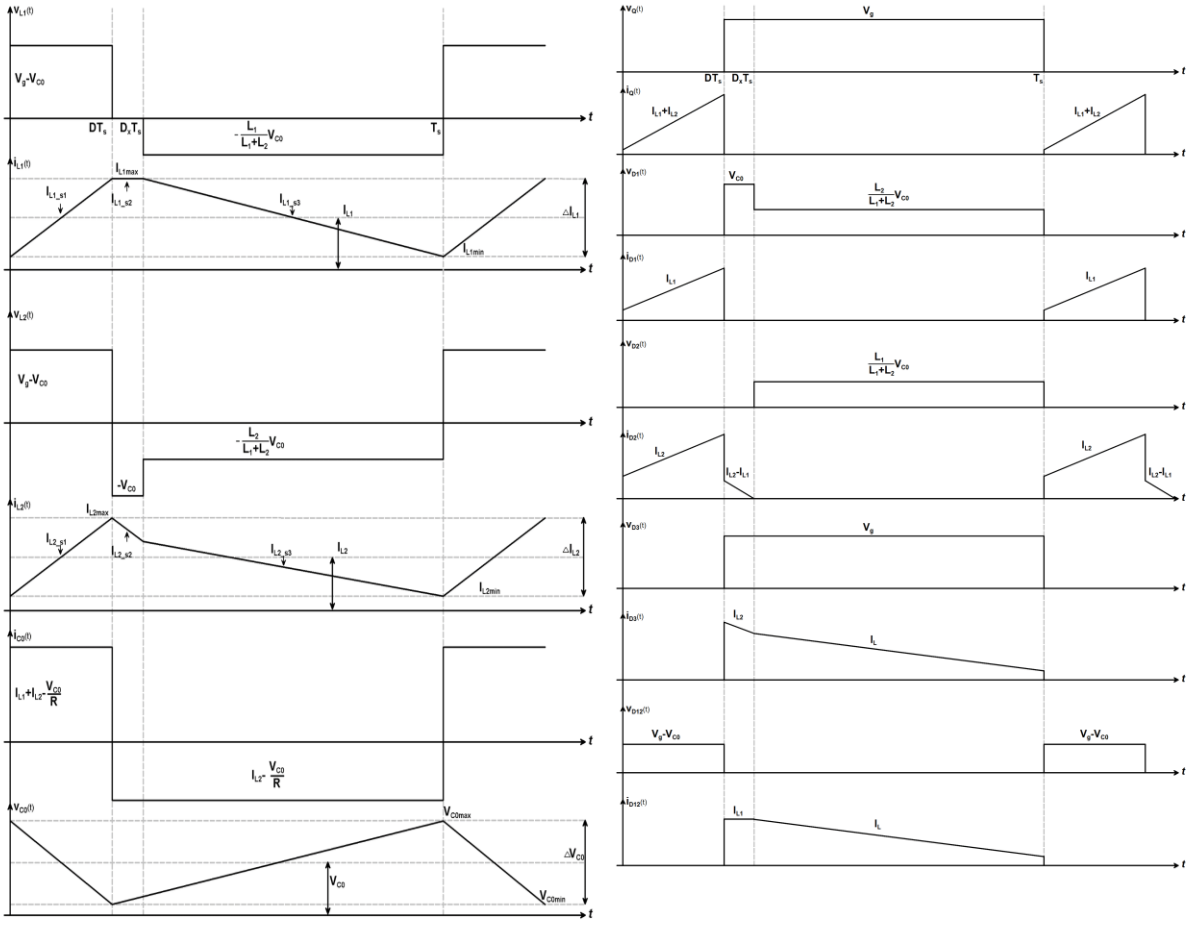

Figure 2.68 The waveforms associated to the reactive components - left and semiconductor devices - right

Simulation and experimental results

The converter operates with the following specifications:

- Input voltage: V_g=24V
- Output voltage: V_o=12V
- Output power: P_o=20W
- Switching frequency: f_s=100kHz

A design procedure for selecting the reactive elements was implemented using MATLAB [54], yielding to inductor L_1=280µH, inductor L_2=140µH, capacitor C_o=33µF, duty cycle D=0.34.

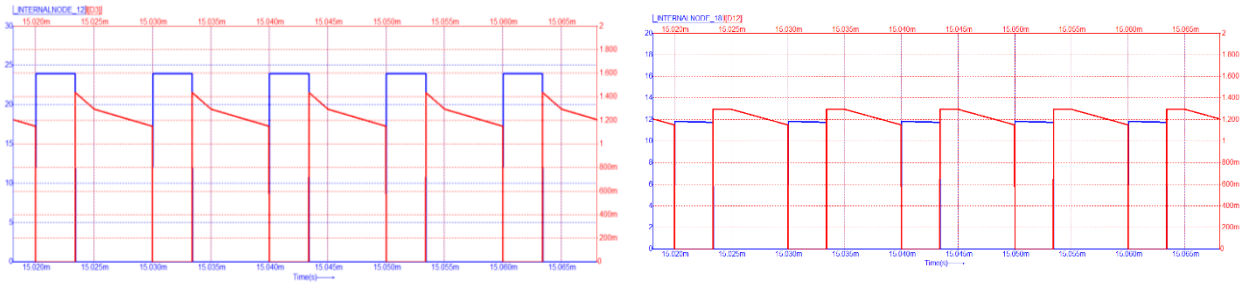

Figure 2.69 Diode D_3 – left, and diode D_{12} – right, currents (red) and voltages (blue).

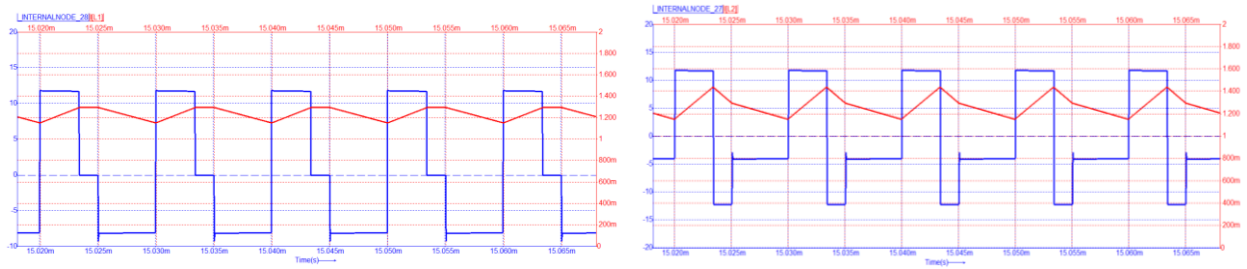

Figure 2.70 Inductor L_1 and L_2 currents (red) and voltages (blue).

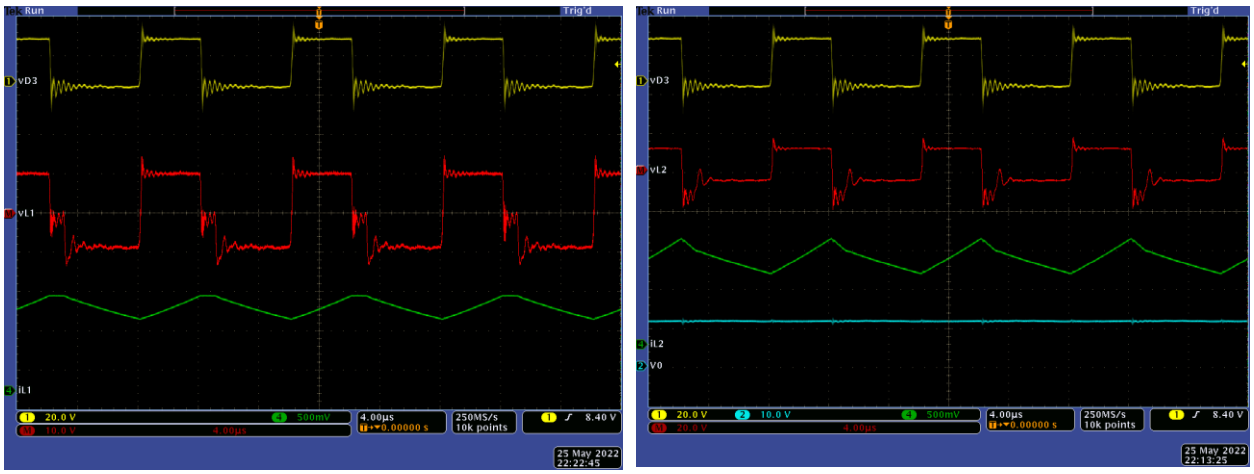

Figure 2.71 Oscilloscope waveforms voltage across D_3 (yellow-v_{D3}); voltage across L_1 (red-v_{L1}); current through L_1 (green- i_{L1}); output voltage on the left, and voltage across D_3 (yellow-v_{D3}) on the right ,voltage across L_2 (red-v_{L2}); current through L_2 (green- i_{L2}); output voltage (light blue -V_0).

These figures capture the essence of the converter operation, and the experimental results for the situation with unequal inductor values demonstrated that inductors imbalance does not impact the static conversion ratio ensuring robust performance.

2.1.1.6 Hybrid Ćuk DC-DC converter with coupled inductors

The paper "A New Hybrid Ćuk DC-DC Converter with Coupled Inductors" [22], introduces a novel hybrid Ćuk-type DC-DC converter with coupled inductors, designed for applications requiring an output voltage higher than the input voltage. The proposed topology achieves an extended static conversion ratio with fewer components than the initial converter from [7], and delivers a higher output voltage at the same duty cycles compared to the classical Ćuk converter, while maintaining negative polarity and reduced output current ripple. Two degrees of freedom in its design allow for enhanced flexibility and performance optimization. Comprehensive *DC* and *AC* analyses, along with evaluations of device stresses, demonstrate its advantages over traditional converters. Simulation and experimental results validated the theoretical predictions, confirming the feasibility of the proposed design in achieving higher conversion efficiency without operating at high duty cycles.

After an introductive section where the state of art of different types of Ćuk converters and their advantages are presented, a description of each section is also documented in [22].

The authors started from the topology of the Ćuk type converter presented in Figure 2.72, [7]. The initial step in designing the proposed converter involved coupling the inductors L_1 and L_2. Assuming ideal coupling, and the transformer ratio n being higher than unity, diode D_3 is always *off* and therefore it can be removed from the circuit. Due to the coupled inductors, simpler and less expensive architecture was achieved with one diode and a magnetic core less, Figure 2.73.

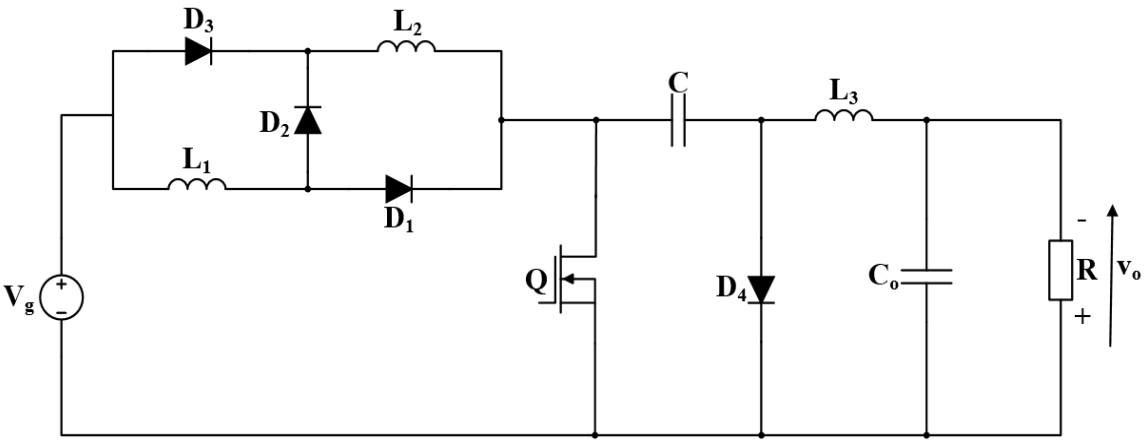

Figure 2.72 The initial Ćuk type step-up converter with the switching cell Up3.

The coupled inductors are modelled using an ideal transformer (*IT*) combined with a magnetizing inductor L_M , as shown in Figure 2.74. In this model, the magnetizing inductor L_M is assumed to be equal to L_1, and all components are considered ideal.

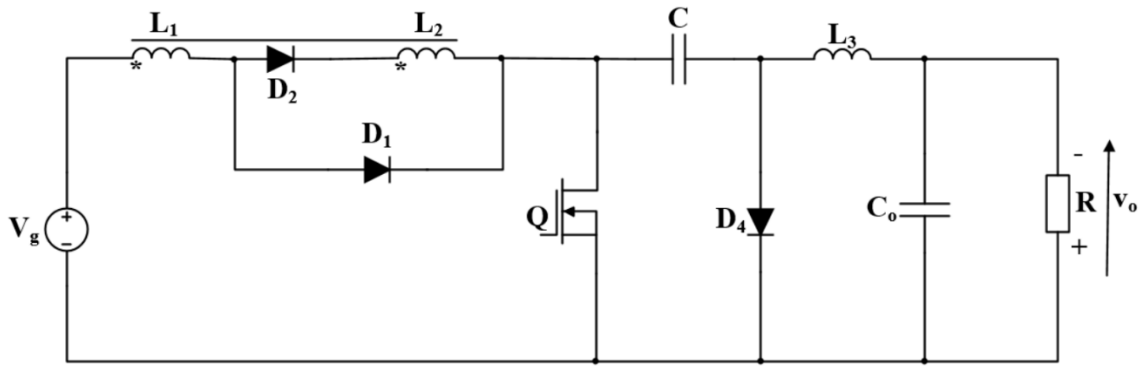

Figure 2.73 The novel proposed hybrid Ćuk-type dc-dc converter with coupled inductors.

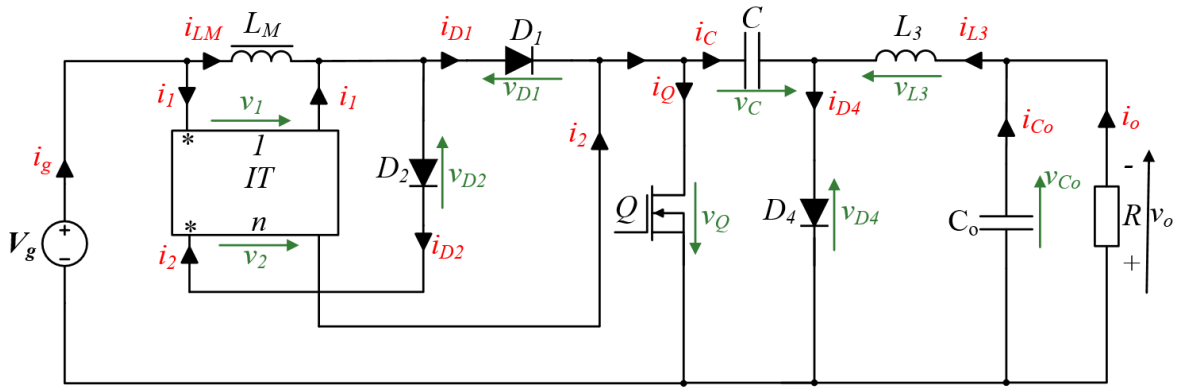

Figure 2.74 Equivalent schematic of the proposed hybrid Ćuk dc-dc converter with coupled inductors.

In CCM, the proposed converter operates with two topological states, based on the status of the power transistor. The switching frequency f_s and period T_s govern the operation, with the duty cycle D controlling the pulse width modulation. During the first state, lasting from 0 to $D \cdot T_s$, transistor Q and diode D_1 conduct, while diodes D_2 and D_4 are reverse-biased. In the second state, occurring from $D \cdot T_s$ to T_s, diodes D_2 and D_4 conduct, while transistor Q and diode D_1 are off. The ideal transformer equations are:

$$\begin{cases} \frac{v_1}{1} = \frac{v_2}{n} \\ i_1 + n \cdot i_2 = 0 \end{cases} \quad (2.26)$$

Small ripple assumptions consider capacitor voltages and inductor currents to be constant, hence equal to their DC values. Analysing the converter, it results that the static conversion ratio is:

$$M = (1 + n \cdot D) \cdot \frac{D}{1-D} \quad (2.27)$$

The duty cycle can be expressed as a function of the static conversion ratio:

$$D = \frac{-1-M+\sqrt{(1+M)^2+4nM}}{2n} \quad (2.28)$$

Examining Equation (2.27), it is observed that the static conversion ratio exceeds unity when the duty cycle is higher than $\frac{\sqrt{1+n}-1}{n}$. For $n = 2$ and $n = 3$, this threshold duty cycle is 0.365 and 0.33, respectively, indicating that the proposed converter allows for both step-up and step-

down conversions. Notably, the step-up region begins at a significantly lower duty cycle compared to the Buck-Boost and Ćuk converters, with the proposed design starting at approximately 0.33 instead of 0.5. As the value of *n* increases, the duty cycle defining the step-up region decreases. Consequently, the step-up region of the proposed converter is broader compared to the Buck-Boost and Ćuk converters. The relationship between static conversion ratios and duty cycles for the classical Ćuk and the proposed topology, at various transformer ratios, is presented in Figure 2.75.

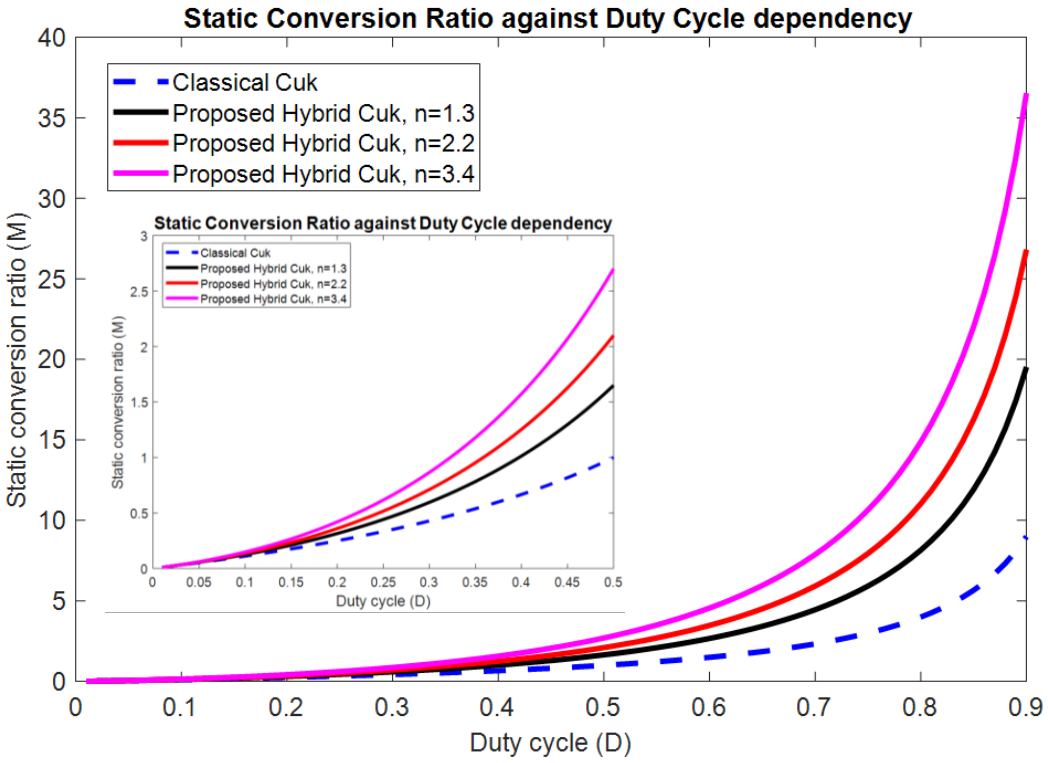

Figure 2.75 Static conversion ratio against duty cycle for the proposed converter (for n = 1.3, 2.2 and 3.4) and for the classical Ćuk converter.

Figure 2.76 and Figure 2.77, illustrate the steady-state waveforms for the reactive components and semiconductor devices. The switching function *q(t)* associated to the transistor is used as a reference, defined as:

$$q(t) = \begin{cases} 1, Q-ON \\ 0, Q-OFF \end{cases} \quad (2.29)$$

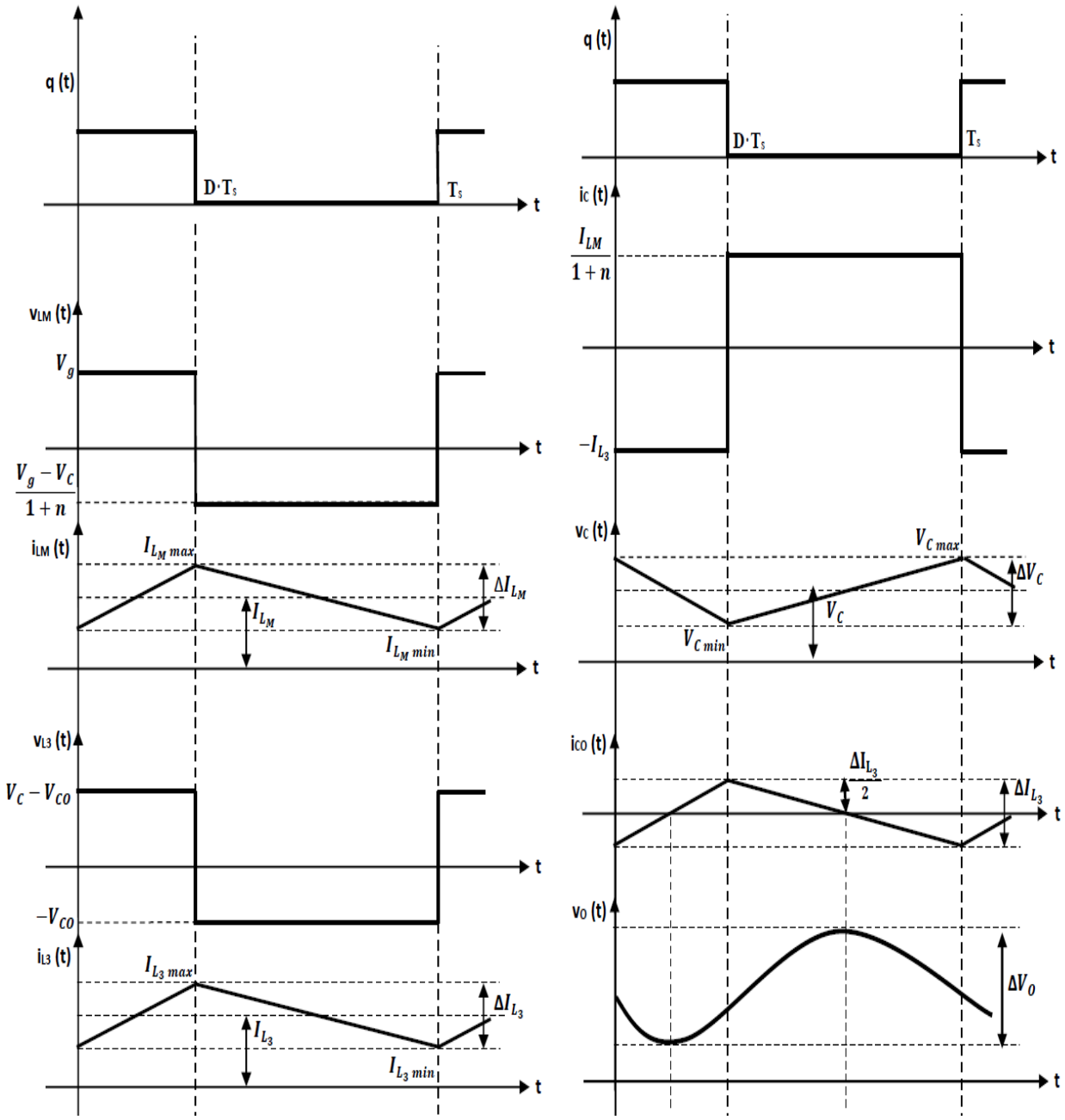

Figure 2.76 Main waveforms associated to the magnetizing inductor L_M and the inductor L_3 - left, and to the internal capacitor C and output capacitor C_o – right.

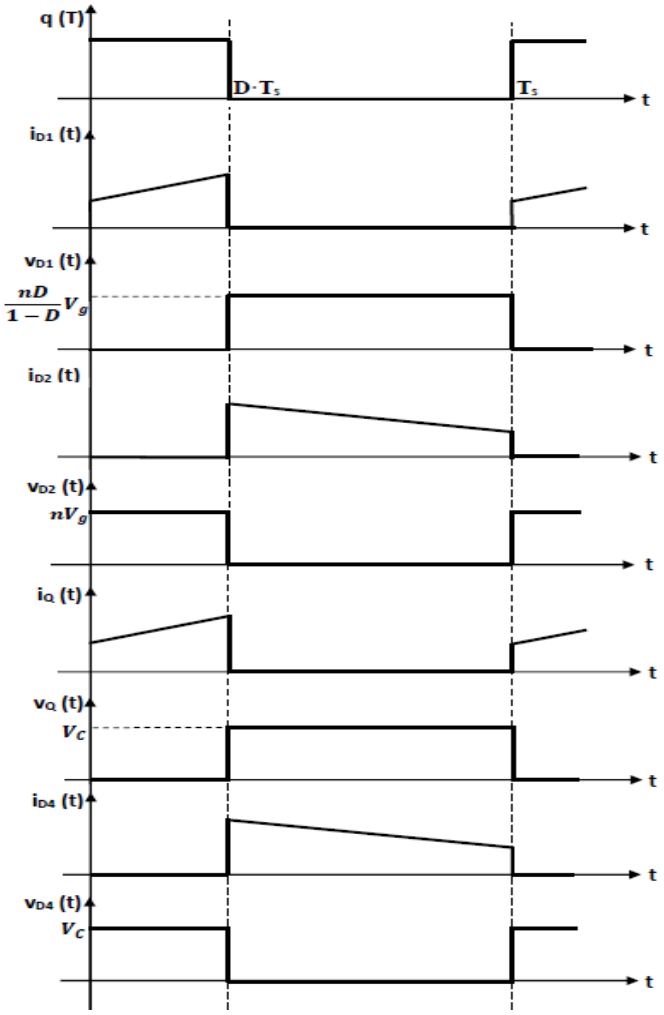

Figure 2.77 Main semiconductor waveforms.

For *CCM* operation, the diodes must remain on during their corresponding topological states, requiring their currents to stay positive. Since the currents through D_1 and D_2 are equal to $i_{LM,}$, the CCM condition mandates that the minimum magnetizing current, $I_{LMmin} = I_{LM} - \frac{1}{2} \cdot \Delta I_{LM}$, must be positive. The final condition is:

$$\frac{2 \cdot L_M \cdot f_S}{R} \geq \frac{(1-D)^2}{D \cdot (1+n \cdot D) \cdot (1+n)} \quad (2.30)$$

The *CCM* condition for diode D_4 is based on the current sum $\frac{i_{LM}}{n+1} + i_{L3}$ that flows through it. Since i_{LM} and i_{L3} share the same monotonicity, the CCM condition is inherently met when

$$\frac{2 \cdot L_e \cdot f_S}{R} \geq \frac{(1-D)^2}{1+n \cdot D} \quad (2.31)$$

where, the equivalent inductor is:

$$L_e = (L_M \cdot (1 + n \cdot D)) || \frac{L_3}{1+n} \quad (2.32)$$

Comparison to similar converter topologies

Table 2.6 compares the proposed hybrid Ćuk DC-DC converter with the classical Buck-Boost, classical Ćuk, and a hybrid Ćuk converter from prior research, assuming identical input voltage V_g, output voltage V_o, and load R. Key parameters compared include the number of components, system order, static conversion ratio M, duty cycle D, and semiconductor stresses.

Table 2.6 Comparison between main parameters of different step-up/down converters.

Parameter	**Type of Converter**			
	Classical Buck-Boost [55]	**Classical Ćuk** [56]	**Hybrid Ćuk** [15]	**Proposed Hybrid Ćuk**
Switches	1	1	1	1
Diodes	1	1	3	3
Total no. of components	4	6	8	8
System order	2	4	4	4
Static conversion ratio-M	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D \cdot (n+D)}{n \cdot (1-D)}$	$\frac{D \cdot (1+n \cdot D)}{1-D}$
Duty cycle-D	$\frac{M}{1+M}$	$\frac{M}{1+M}$	$\frac{A - n \cdot (1+M)}{2}$	$\frac{B-(1+M)}{2n}$
Switch current stress	$M^2 \cdot \frac{V_g}{R}$	$M \cdot (1+M) \cdot \frac{V_g}{R}$	$M^2 \cdot \frac{V_g}{R}$	$M^2 \cdot \frac{V_g}{R}$
Switch voltage stress	$(1+M) \cdot V_g$	$(1+M) \cdot V_g$	$\frac{2 \cdot M \cdot V_g}{-n - n \cdot M + A}$	$\frac{2nM \cdot V_g}{-1 - M + B}$
Maximum diode dc current stress	$M^2 \cdot \frac{V_g}{R}$	$M \cdot (1+M) \cdot \frac{V_g}{R}$	$M \cdot \frac{V_g}{R}$	$M \cdot \frac{V_g}{R}$
Maximum diode voltage stress	$(1+M) \cdot V_g$	$(1+M) \cdot V_g$	$\frac{2 \cdot M \cdot V_g}{-n - n \cdot M + A}$	$\frac{2nM \cdot V_g}{-1 - M + B}$

where, $A = \sqrt{n^2(1+M)^2 + 4\mathrm{nM}}$, $B = \sqrt{(1+M)^2 + 4nM}$

Unlike the classical Ćuk, the proposed converter includes two additional diodes but achieves lower current stresses through the transistors and diodes, while maintaining the same system order. As shown in Figure 2.75, the proposed topology achieves a higher static conversion ratio at the same duty cycle, making it more suitable for step-up applications requiring significant input-to-output voltage differences.

Design example

The design objective is to develop a hybrid Ćuk converter based on the following specifications:

- Input voltage: V_g= 24-36V
- Output voltage: V_o=120V
- Output power: P_o=30-50W
- Switching frequency: f_s=100 kHz

Knowing the design specifications, the components value were calculated, using the equations presented in [22].

The minimum and maximum values of the static conversion ratio are M=3.33 - 5. With D_{min}=0.6, corresponding to the minimum static conversion ratio, the required turns ratio results in n=2.03. The maximum duty cycle, that corresponds to maximum static conversion ratio is D_{max}=0.68. The maximum and minimum load resistances are determined by the minimum and maximum output power, respectively and the values are R_{min}=288Ω and R_{max}=480Ω. The minimum magnetizing inductor value (L_{Mmin}) was calculated as 492.9 µH under worst-case conditions (maximum load resistance and input voltage), with L_1=L_M=492.9 µH and L_{2min}=$n^2 \cdot L_{Mmin}$=2.03 mH.

For the practical implementation, L_M=773.38 µH was used. The minimum inductor L_{3min} was found to be 3.1 mH, and a practical value of L_3=3.45 mH was selected. The internal capacitor was designed to limit the voltage ripple to 5%, resulting in a standard value of 33 µF, while the output capacitor, with a 10% voltage ripple limit, was chosen as 3.3 µF. The transistor voltage stress was calculated as V_Q=210 V, with an average current of I_Q=1.5 A. Diode stresses showed a maximum voltage of V_D=210 V and a maximum DC current of I_D=1.2 A.

Simulations and experimental results

To validate the theoretical analysis of the ideal hybrid Ćuk converter, simulations were conducted using the Caspoc tool, [50]. The parameters matched the practical prototype specifications: V_g = 35 V, L_1 = 773.38 µH, L_2 = 2.39 mH, L_3 = 3.45 mH, C = 33 µF, C_0 = 3.3 µF, R = 360 Ω, f_s = 100 kHz. A slight adjustment to the transformer ratio yielded n=1.758, leading to a calculated duty cycle of D=0.621. The simulations confirmed a DC output voltage V_O, consistent with theoretical expectations, as depicted in Figure 2.78.

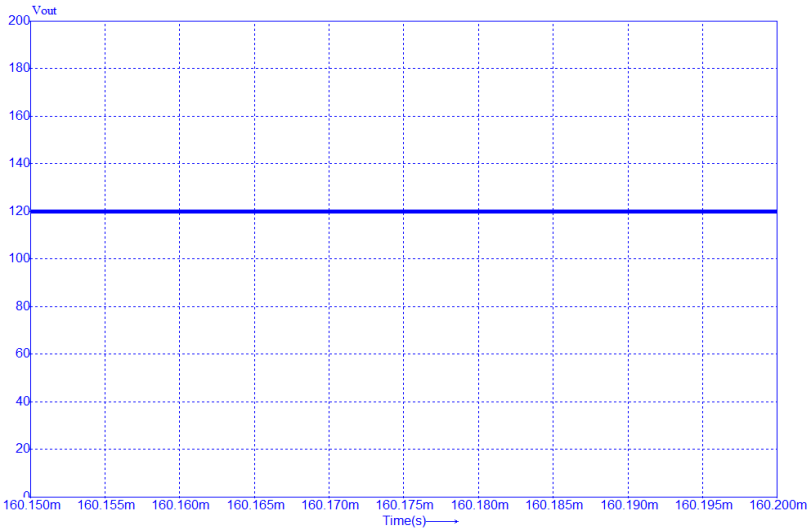

Figure 2.78 Caspoc simulation. Output dc voltage.

The implemented prototype employs the parameters outlined in the design example. The setup included a fixed input voltage, $V_g = 35$ V, a switching frequency $f_s = 100$ kHz, and load $R = 360\ \Omega$. The chosen transistor was Infineon MOSFET STW37N60DM2AG and diodes $D_{1,2,4}$, RFN10NS6SFH. In all the recorded waveforms, the oscilloscope reference signal was set to the drain-to-source voltage of transistor Q. For a duty cycle of $D = 0.2$, the operation was in *DCM* for diodes D_1 and D_2, as verified by Equation (2.30) and shown in Figure 2.79. At $D = 0.66$, Figure 2.80 and Figure 2.81 enface the expected rectangular inductor voltage waveforms and triangular inductor current waveforms, consistent with both theoretical and simulated results.

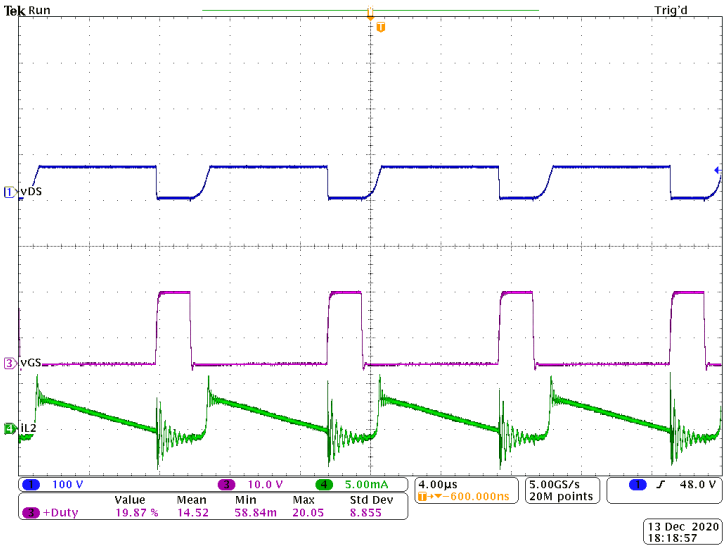

Figure 2.79 Oscilloscope waveforms: drain-to-source voltage (dark blue- v_{DS}); gate-to-source voltage (purple- v_{GS}); current through L_2 at the duty cycle $D = 0.2$.

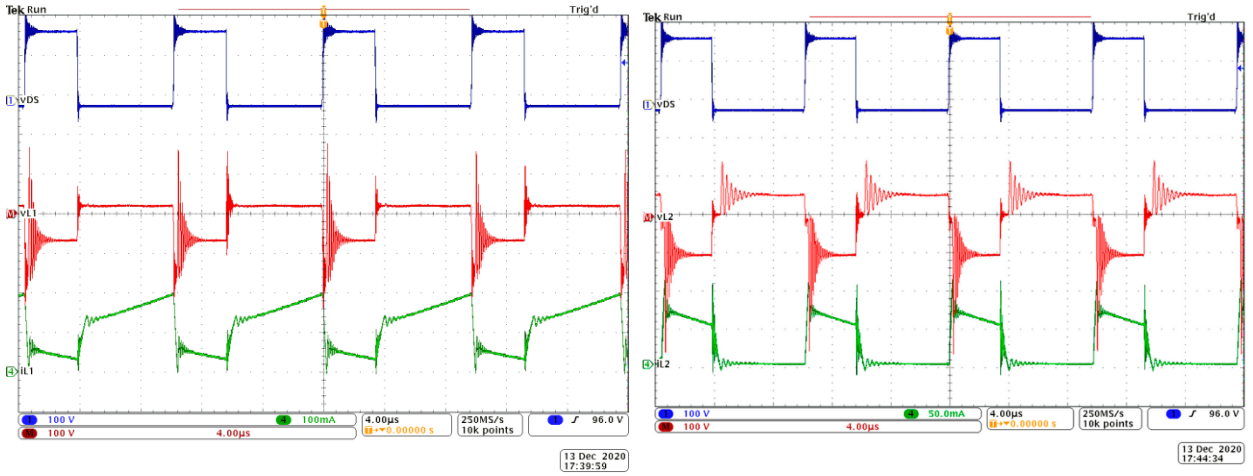

Figure 2.80 Oscilloscope waveforms: drain-to-source voltage (dark blue- v_{DS}); voltage across the primary (red- v_{L1}); the primary current L_1 (green- i_{L1}) – left and drain-to-source voltage (dark blue-v_{DS}); voltage across the secondary L_2 (red-v_{L2}); secondary current (green-i_{L2}) - right. Duty cycle $D = 0.66$.

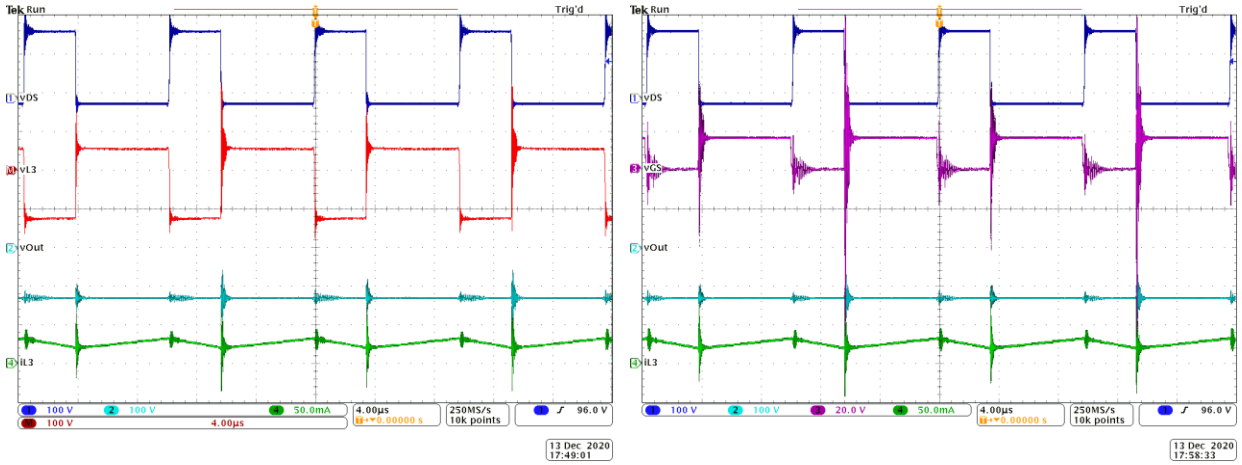

Figure 2.81 Oscilloscope waveforms: drain-to-source voltage (dark blue-v_{DS}); voltage across L_3 (red-v_{L3}); output voltage (light blue-V_O) and current through L_3 (green-i_{L3}) – left; and drain-to-source voltage (dark blue-v_{DS}); gate-to-source voltage (purple); output voltage (light blue-V_O), current through L_3 (green-i_{L3}) - right. Duty cycle $D = 0.66$.

The static conversion ratio of the prototype was evaluated by varying the duty cycle D and measuring the output voltage V_o. Figure 2.82 – left, shows the comparison of the ideal, theoretical (with conduction losses), and measured conversion ratios, with close match up to D=0.6 and deviation at higher duty cycles, typical to step-up converters. Figure 2.82 – right, highlights the theoretical conversion ratios peak value and subsequent decline at very high duty cycles due to the finite maximum attainable ratio. Figure 2.83 illustrates the efficiency dependence on output power at a constant V_o=120 V.

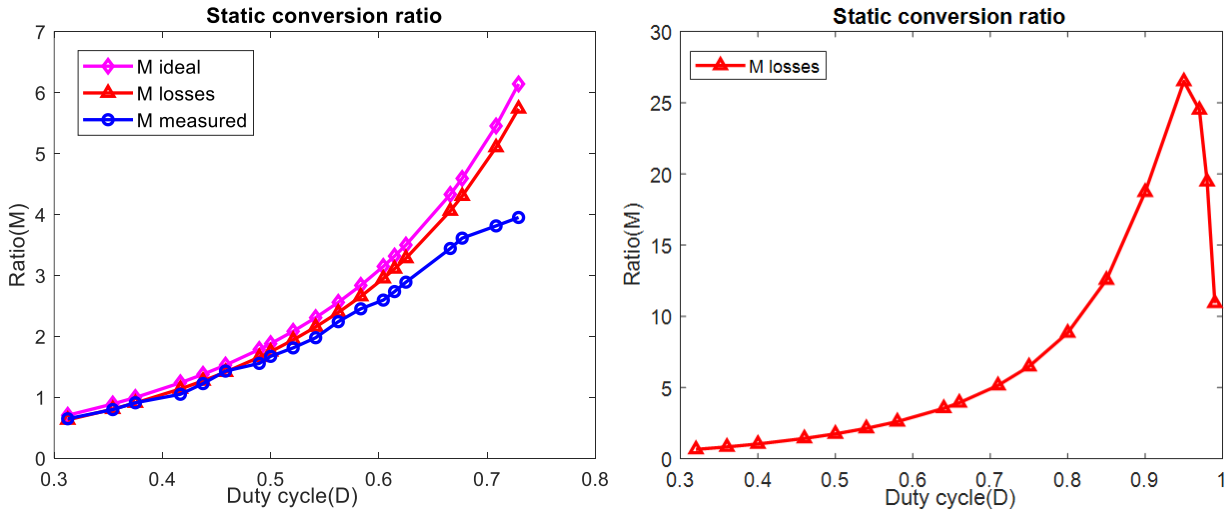

Figure 2.82 The experimental static conversion ratio against the duty cycle (blue) compared to the ideal one (purple) and the theoretical one in the presence of conduction losses (red) – left, and the theoretical dependency of the static conversion ratio on the duty cycle in the presence of losses considering an extended duty cycle range, revealing the maximum attainable dc gain - right.

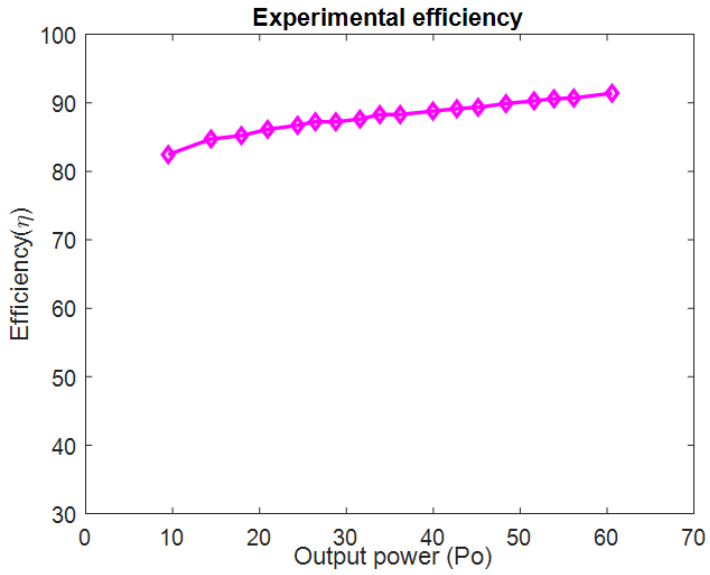

Figure 2.83 The experimental efficiency against the output power.

The simulation results presented in [22] and the experimental results validated the theoretical considerations both qualitatively and quantitatively, demonstrating consistency in *DC* currents, *DC* voltages, and peak-to-peak ripples with all measured values, aligning with the theoretical predictions. Despite deviations at higher duty cycles, the close agreement between the experimental and theoretical curves in the mid-range demonstrates the robustness and accuracy of the proposed converter under typical operating conditions and the efficiency curve demonstrates the features of the proposed converter under practical conditions. This work was supported by a grant of the Romanian Ministry of Education and Research, CNCS-UEFISCDI, project number

PN-III-P1-1.1-PD-2019-1006, within PNCDI III, PD 76/2020, [43] in which the author was a director.

Another structure of a hybrid Ćuk converter, [15], was designed to achieve a wide step-up and step-down voltage conversion ratio with reverse output polarity relative to the input voltage. The authors proposed a topology [15] that improves by extending the voltage conversion range and simplifies the design upon the classical Ćuk converter and existing hybrid versions. The authors started from the topology of the Ćuk converter presented in Figure 2.72, [7], coupled the inductors, but this time the transformer ratio was considered lower than unity. The complete analyses can be found in [15], and the simulations together with the practical implementation of the circuit validated the accuracy of the theoretical model.

2.1.1.7 Hybrid Boost-L and Buck-L converters with coupled inductors and less than unity transformer ratio

From the grant, [42], the research for another family of converters was funded. The architecture of the converter was derived from a deep analysis of the step-up hybrid Boost-L converter with switching structure Up3 from [7]. In this study, coupled inductors were employed, and the transformer ratio was set to be less than unity. Using the fundamental converter cell rotation principle [53], six converters were obtained: two boost, two buck, and two buck-boost types. Among these, only topologies with a single transistor and three diodes were investigated, while the configurations with three transistors and one diode were excluded. The Boost-*L* converter structure and analysis are detailed in the paper [19], highlighting the potential benefits and suitability of the hybrid inductor-based design for photovoltaics, and a summary is provided in the application section.

The Buck-*L* converter obtained from the same family, is described in [14]. This step-down DC-DC converter topology was developed, featuring a simplified second-order system that facilitates easier design and control compared to higher-order converters. The design is cost-efficient, incorporating one transistor, three diodes, and coupled inductors on a shared magnetic core. This converter achieves high efficiency, exceeding 90% at duty cycles above 0.2, as confirmed through theoretical analysis, simulations, and experimental results. Unlike traditional Buck converters that require higher duty cycles, it maintains strong performance and efficiency even at moderate duty cycles. A prototype was built and tested. Experimental results showed an output voltage ripple below 1%, validating the theoretical predictions. The converter operates with lower voltage and current stresses on components compared to other advanced step-down converters, while its compact structure reduces the total component count relative to more complex topologies like quadratic or stacked Buck converters. This converter is particularly suitable for applications requiring small step-down voltage adjustments, such as battery management in electric vehicles and renewable energy systems, [14].

2.1.1.8 Other publications

Several publications were co-authored in collaboration with colleagues from the Applied Electronics Department, incorporating specific novelty from the study. *A novel stacked step-down switching converter* is presented in [10], as a solution for applications where a small difference between the input and output voltages is needed. This topology use only one transistor and two

diodes, with equal inductors, allowing for coupling and achieving zero ripple current in inductor L_1, thereby reducing filtering demands. It features lower semiconductor voltage and current stresses compared to other topologies.

The research paper "*A Generalized Model for Single-Switch Stacked Step-Down Converters*", [24] further extends the concept by presenting a generalization of stacked step-down converters, moving beyond the two-stage design to an arbitrary number of stages. The study focuses on optimizing step-down ratios close to unity, where classical buck converters require impractically high duty cycles. The results are supported by both simulations and experimental validation, confirming the feasibility of the proposed designs. This work is significant, as it offers a scalable and efficient solution for DC-DC conversion, enhancing the performance and applicability of power electronics in various fields.

Originated from the same switching cell in [10], a new converter is derived by rotating the switching cell between source, common point and ground. Within this family, *a stacked step-up architecture* is presented in [12]. This converter exhibits a higher step-up conversion and lower voltage stresses compared to the classical boost.

The paper [20], presents a *boost converter design with two independently controlled switches*, achieving a higher static conversion ratio compared to traditional configurations, cascaded, multiphase and quadratic converters. The converter is derived from the buck-cascaded-by-boost (BuCBB) converter, [57], using the basic cell rotating concept and switch synthesis, [53]. This converter stands out by maintaining moderate duty cycles while achieving significant voltage step-up, making it suitable for applications requiring high voltage gain. A comprehensive analysis, including *DC* and *AC* characteristics, device stresses, and design equations is provided alongside simulations that validated the theoretical predictions. The novelty lies in its innovative topology, which employs two transistors and two diodes and operates with three topological states, offering an improvement in static conversion ratio compared to the double cascade boost converter if the duty cycle is properly chosen. Experimental results further confirmed the feasibility and effectiveness of the proposed design and its potential in high step-up voltage applications.

Starting from the same buck-cascaded-by-boost (BuCBB) converter [57], and using the basic cell rotating concept and switch synthesis, [53], the proposed *buck-boost topology* is derived, [21]. This converter features two independently controlled active switches, capable of operating either as a boost or as a buck converter depending on input-output conditions while switching at moderate duty cycles. It incorporates a second-order *LC* filter and uses the integrated magnetic concept for the coupled inductors, achieving a nearly *DC* output inductor current and reducing filtering requirements. One degree of freedom is gained using coupled inductors and also the order of the converter is decreased by one, due to this. A *DC* analysis is conducted to derive the static characteristics of the converter, along with design equations to support its practical implementation. Simulations and experimental results are performed.

Another family of converters with coupled inductors are found and analysed in three distinct papers, [23], [31], [35]. In paper [23], the *step-up converter with a coupled inductor*, one active switch, and three diodes, operating as a Boost converter is introduced. This design achieves a higher static conversion ratio at the same duty cycle compared to a traditional Boost converter,

making it suitable for applications requiring significantly higher output voltages than the input. The converter operating principles, steady-state equations, and design equations are detailed. Simulation and experimental results confirm the theoretical analysis, validating the feasibility and effectiveness of the proposed topology, which offers high voltage gain at moderate duty cycles due to its two degrees of freedom.

The *fourth-order Buck-Boost converter* featuring coupled inductors, one MOSFET, three diodes, two capacitors, and a separate inductor is presented in [31]. This design has two degrees of freedom, enabling significantly higher output voltage compared to classical Buck-Boost converters at the same duty cycle. The converter *DC* and *AC* characteristics are analyzed, with design equations provided. The functionality is validated through simulations and practical experiments in open-loop operation. A state-space model is derived to calculate the control-to-output transfer function, which is approximated by a second-order function with 99.34% accuracy for easier controller design. The converter operation in CCM is analyzed, providing guidelines for designing the reactive elements and selecting semiconductor components based on voltage and current stresses. The proposed converter offers superior step-up/step-down capabilities, and future work aims to explore other fourth-order topologies using others switching cell configurations.

The last converter analysed from this family is a *fourth-order step-down converter*, [35]. After analysing the converter, the paper focuses on designing a controller for this fourth-order step-down converter, beginning with the derivation of the control-to-output transfer function using a state-space model. This fourth-order function is approximated by a second-order transfer function using the *tfest* function, ensuring high accuracy in the low-frequency domain. A type III error amplifier is then designed for the second-order model using conventional pole-zero placement method. The theoretical analysis is validated through simulations, demonstrating the system stability and fast response to changes in the input voltage and load. The study highlights the effectiveness of transfer function approximation for simplifying controller design in high-order converters.

A *step-down hybrid quadratic converter* derived from the quadratic Buck-Boost converter, [58], designed for applications requiring high step-down voltage difference between input and output is presented in [34]. A *DC* analysis was performed, validated through CASPOC simulations and practical experiments, showing good agreement with theoretical predictions. The converter achieves a lower output voltage than a conventional buck converter at the same duty cycle.

Part of the same family, *the quadratic step-up DC-DC converter* using a single transistor and three diodes, designed for applications requiring a low step-up voltage difference is described in [28]. Compared to traditional step-up converters, the proposed topology exhibits lower voltage and current stresses, improving efficiency and reducing cost. The operation principle, steady-state analysis, and design equations are detailed, with computer simulations and experimental validation confirming its feasibility.

From the same category of *step-down converters,* in [25] a new structure is presented. This architecture started from a high voltage gain SEPIC converter used for renewable energies applications, [59]. The new quadratic step-down converter is designed to achieve an extreme low conversion ratio while maintaining a moderate duty cycle. It features a single active switch,

simplifying the control mechanism, and maintains high efficiency by minimizing conduction and switching losses. Both simulation and experimental results validated the feasibility and effectiveness of this new topology, making it a promising solution for automotive, telecommunications, and renewable energies sectors. This paper was partially supported by the grant of the Romanian Ministry of Education and Research, CNCS-UEFISCDI, project number PN-III-P1-1.1-PD-2019-1006, within PNCDI III, PD 76/2020, [43], in which the author was conducting the grant.

From the same switching cell, in [60] a *novel buck-boost converter* is proposed, capable of both increasing and decreasing the output voltage. It offers an extended step-up capability over a large range, while the step-down function is limited to a narrower interval. For duty cycles exceeding 0.59, it surpasses the static conversion ratio of conventional boost converters, providing enhanced efficiency and suitability in high-voltage applications, [60].

From the same grant, [43], *a single-switch step-down DC-DC converter*, that introduces significant improvements over conventional buck converter topologies, is presented in [29]. The proposed structures feature a single active switch and two diodes, achieving smoother input current and enhanced efficiency across a wide range of duty cycles. Unlike traditional buck converters, that suffer from increased power losses and degraded efficiency when operating at low step-down voltage ratios, the proposed topology is optimized for applications requiring a moderate step-down conversion, making it particularly suitable for renewable energies systems, battery-powered applications, electric vehicles, and DC-link voltage regulation.

Efficient power conversion is essential in modern electronics, particularly in applications requiring a small voltage difference between the input and output. Addressing this need, *a new buck-type DC-DC converter* has been developed and presented in [26], offering a higher static conversion ratio compared to the conventional step-down designs, while maintaining efficiency above 90% over a large range of duty cycles. This new topology, [61], features one active switch and two diodes, optimizing component stresses while ensuring improved performance. It is particularly well-suited for applications where the output voltage is lower but remains close to the input voltage, such as photovoltaic systems, battery-powered devices, and electric vehicles.

In [27], *a step-down quadratic converter* is proposed, offering an output voltage slightly lower than the input voltage while minimizing component stress. This topology, that incorporates one active switch and three diodes, ensures efficient power conversion with enhanced performance over a broad duty cycle range. Compared to a classical buck converter the static conversion ratio at the same duty cycle D is higher, it provides improved efficiency and better control on the output voltage.

A novel *switched-capacitor step-up DC-DC converter* featuring smooth output current, a single active switch, and four diodes is analysed in [33]. Unlike the classical boost converter, it achieves a lower conversion ratio at the same duty cycle, making it suitable for applications requiring small voltage step-up. It achieves approximately 90% efficiency over a wide duty cycle range. The analysis extends to scenarios with *unequal capacitor values*, deriving the key equations and semiconductor stresses. Simulation and experimental testing of the prototype validated the theoretical and simulation results, confirming the expected performance.

Starting from the paper presented in [62], extracting the switching cell and applying the switching cell rotation technique [53], a *cubic buck-boost converter with a higher step-up voltage conversion* compared to classical buck-boost and boost converters is obtained. The analysis of the converter presented in [63], highlighted superior efficiency, reduced conduction losses, and enhanced voltage regulation, proving the advantages of the proposed topology. This research establishes a new high-performance approach to buck-boost power conversion, providing a foundation for future advancements in high-gain DC-DC converters.

From the same switching cell [62], *a novel single-switch cubic buck converter* that achieves a higher static conversion ratio than existing buck, quadratic, and cubic topologies, providing a higher output voltage at the same duty cycle is described in the extended paper presented in [36]. This converter, despite its increased number of components, maintains a simple control structure using a single transistor. The research compared the proposed topology with several existing buck-type converters, revealing its advantages in terms of reduced transistor stress and higher conversion efficiency.

2.1.2 Control methods for dc-dc converters

2.1.2.1 Stability analysis of a two-phase boost converter

The paper [17], addresses the exact stability analysis of a two-phase boost converter, a critical topic in power electronics where stability analysis is crucial for designing reliable systems. The proposed methodology enhances the understanding of the system dynamic behaviour, offering an analytical solution that surpasses existing empirical or simplified approaches. The research was partially supported by research grants PCD-TC-2017, [42], which was conducted by the candidate.

The article [11], includes an analysis of the single-phase converter, which the authors utilized to validate its functionality prior to extending the topology to the two-phase configuration [18]. The schematic of the two-phase Boost converter is presented in the Figure 2.84, along with a proportional-type controller. In this configuration, the difference between the reference voltage and the output voltage is amplified by a factor k and subsequently compared to a sawtooth carrier signal.

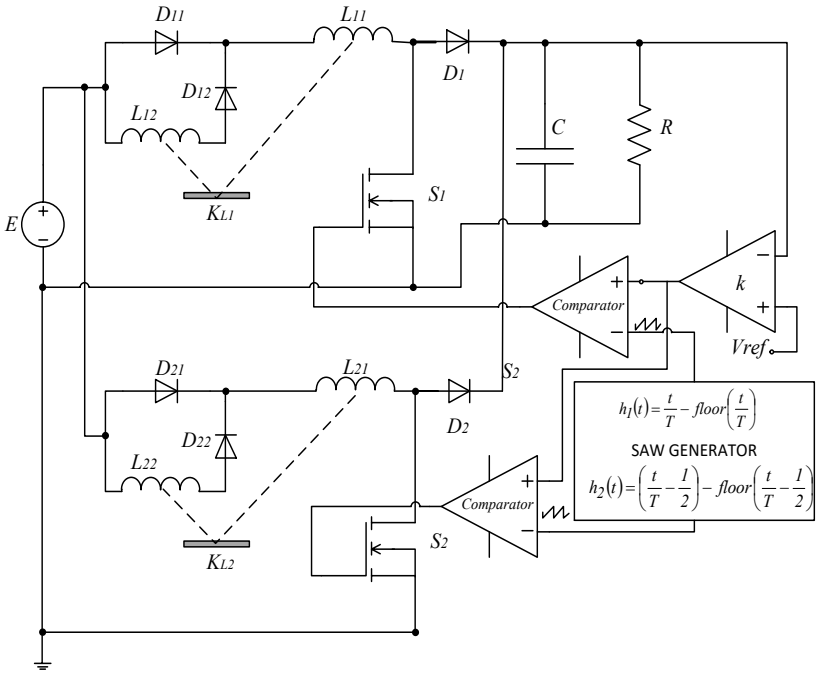

Figure 2.84 The schematic of a two-phase Boost converter.

The static conversion ratio of the converter is:

$$M = \frac{1+n \cdot D}{1-D} \qquad (2.33)$$

In Figure 2.84, the sawtooth generator produces a ramp signal with maximum and minimum values of $V_U=1$ and $V_L=0$, respectively. Two identical sawtooth carriers, phase-shifted by 180°, set the switching frequency for each transistor. Figure 2.85, illustrates the pulse-width modulated (PWM) control signals, showing that the gate signals are shifted by 180°, and each transistor duty cycle is less than 0.5 to prevent simultaneous conduction.

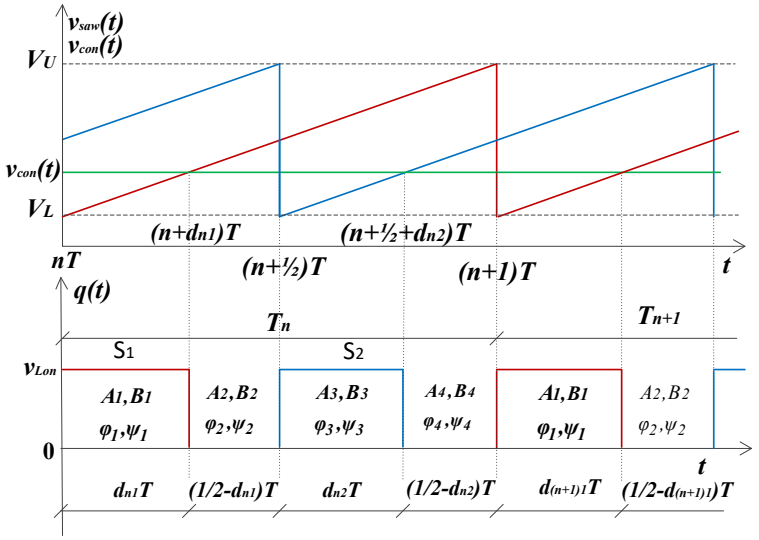

Figure 2.85 PWM signals that control the transistors.

The proposed discrete model is characterized by a system of *n+1* equations. One equation provides a recurrence relation for the state vector, while the remaining *n* equations correspond to non-dynamical constraints for controlling each converter. These equations include a bifurcation parameter $P_{bif.}$, used to identify the instability threshold, as detailed in previous studies [64] - [65]. The developed theoretical studies exhibit a high degree of generality, making them well-suited for the two-phase converter, with certain modifications to accommodate its specific operation principles. While the analysis focuses on the two-phase converter, the approach can be seamlessly extended to multiphase architectures.

In the case of a two-phase converter, the recurrence equation along with the two non-dynamical constraints can be expressed in the most general form as follows:

$$\begin{cases} x_{n+1} = g(x_n, u_n, d_{n1}, d_{n2}, p_{bif}) \\ F_1(x_n, u_n, d_{n1}, d_{n2}, p_{bif}) = 0 \\ F_2(x_n, u_n, d_{n1}, d_{n2}, p_{bif}) = 0 \end{cases} \quad (2.34)$$

The first equation represents the discrete state equation, while the other two equations describe the control constraints. The control voltage is set to be equal to the sawtooth ramps at the moments when the *off* switching takes place. The variables x_n, u_n, d_{n1}, d_{n2} in (2.34) represent the state vector, input vector, and the duty cycles of transistors 1 and 2, respectively. The converter cycles through four distinct topological states. The state matrices and transition matrices denoted by A_i, B_i and φ_i, ψ_i by specific symbols for each topological state, $i = \overline{1,4}$, are defined based on these operational states. The relationships that define these matrices are outlined as follows:

$$\begin{aligned} &\left.\begin{matrix} \varphi_1 = e^{A_1 d_{n1} T} \\ \psi_1 = A_1^{-1}(\varphi_1 - I)B_1 \end{matrix}\right\}, && t \in [nT, nT + d_{n1}T) \\ &\left.\begin{matrix} \varphi_2 = e^{A_2\left(\frac{1}{2} - d_{n1}\right)T} \\ \psi_2 = A_2^{-1}(\varphi_2 - I)B_2 \end{matrix}\right\}, && t \in [nT + d_{n1}T,\ nT + T/2) \\ &\left.\begin{matrix} \varphi_3 = e^{A_3 d_{n2} T} \\ \psi_3 = A_3^{-1}(\varphi_3 - I)B_3 \end{matrix}\right\}, && t \in [nT + T/2, nT + T/2 + d_{n2}T) \\ &\left.\begin{matrix} \varphi_4 = e^{A_4\left(\frac{1}{2} - d_{n2}\right)T} \\ \psi_4 = A_4^{-1}(\varphi_4 - I)B_4 \end{matrix}\right\}, && t \in [nT + T/2 + d_{n2}T,\quad nT + T) \end{aligned} \quad (2.35)$$

By recursively expressing the state vector at the end of each topological state in terms of its value at the beginning of the same state, the function *g* in equation (2.34) is derived.

$$g(x_n, u_n, d_{n1}, d_{n2}, p_{bif}) = \varphi_4\varphi_3\varphi_2\varphi_1 x_n + (\varphi_4\varphi_3\varphi_2\psi_1 + \varphi_4\varphi_3\psi_2 + \varphi_4\psi_3 + \psi_4)E \quad (2.36)$$

From the previous equation, the steady-state state vector is determined by imposing the conditions $x_{n+1} = x_n = X$, $d_{n1} = D_1$ and $d_{n2} = D_2$. It results that:

$$X = (I - \Phi_4\Phi_3\Phi_2\Phi_1)^{-1}(\Phi_4\Phi_3\Phi_2\Psi_1 + \Phi_4\Phi_3\Psi_2 + \Phi_4\Psi_3 + \Psi_4)E \quad (2.37)$$

The capital letters represent the transition matrices evaluated at the steady-state operating point.

The control functions of the two-phase converter

The control voltage equals the two ramp signals at the time moments, $(n+d_{n1})T$, and $(n+1/2+d_{n2})T$. By applying the equations of the ramps and recognizing that the control voltage corresponds to $k\left[V_{ref}-v_o(t)\right]$, the two control functions F_1, F_2 are derived as:

$$\begin{cases} F_1(x_n,d_{n1},d_{n2},E,k)=k\left[V_{ref}-V_o(nT+d_{n1}T)\right]-\frac{V_U-V_L}{T}d_{n1}T-V_L \\ F_2(x_n,d_{n1},d_{n2},E,k)=k\left[V_{ref}-V_o(nT+T/2+d_{n2}T)\right]-\frac{V_U-V_L}{T}d_{n2}T-V_L \end{cases} \quad (2.38)$$

The output voltage $v_o(t)=v_C(t)$, is expressed in terms of the state vector using an extracting vector, v_{exv}. The state vector at time moments other than the beginning of the period can be written as a function of the state vector at the beginning of the period. By substituting all these relationships into equations (2.38), the control functions F_1 and F_2 are obtained in the following form:

$$\begin{cases} F_1(x_n,d_{n1},d_{n2},E,k)= \\ k\left[V_{ref}-v_{exv}(\varphi_1 x_n+\psi_1 E)\right]-(V_U-V_L)d_{n1}-V_L \\ F_2(x_n,d_{n1},d_{n2},E,k)= \\ k\left\{V_{ref}-v_{exv}[\varphi_3\varphi_2\varphi_1 x_n+(\varphi_3\varphi_2\psi_1+\varphi_3\psi_2+\psi_3)E]\right\}-(V_U-V_L)d_{n2}-V_L \end{cases} \quad (2.39)$$

Exact stability analysis of the two-phase boost converter

By performing a small-signal analysis through the linearization of equations (2.36) and (2.39), the duty cycles d_{1n} and d_{2n} are eliminated, and the Jacobian $J_g(X)=\left.\frac{\partial g}{\partial x_n}\right|_{x=X}$ is computed, ultimately leading to the following result:

$$J_g(X)=\left.\frac{\partial g}{\partial x_n}\right|_{\cdot}-\left.\frac{\partial g}{\partial d_{n1}}\right|_{\cdot}\left(\left.\frac{\partial F_1}{\partial d_{n1}}\right|_{\cdot}\right)^{-1}\left.\frac{\partial F_1}{\partial x_n}\right|_{\cdot}+\left.\frac{\partial g}{\partial d_{n2}}\right|_{\cdot}\left(\left.\frac{\partial F_2}{\partial d_{n2}}\right|_{\cdot}\right)^{-1}\left[\left.\frac{\partial F_2}{\partial d_{n1}}\right|_{\cdot}\left(\left.\frac{\partial F_1}{\partial d_{n1}}\right|_{\cdot}\right)^{-1}\left.\frac{\partial F_1}{\partial x_n}\right|_{\cdot}-\left.\frac{\partial F_2}{\partial x_n}\right|_{\cdot}\right] \quad (2.40)$$

The vertical bar indicates that the corresponding partial derivatives are evaluated in the operating point, which must be determined using equations (2.37) to (2.39), under steady-state conditions, $d_{n1}=D_1$ and $d_{n2}=D_2$. Consequently, the following system must be solved for X, D_1, D_2:

$$\begin{cases} X=(I-\Phi_4\Phi_3\Phi_2\Phi_1)^{-1}(\Phi_4\Phi_3\Phi_2\Psi_1+\Phi_4\Phi_3\Psi_2+\Phi_4\Psi_3+\Psi_4)E \\ F_1(X,D_1,D_2,E,k)=k\left[V_{ref}-v_{exv}(\Phi_1 x_n+\Psi_1 E)\right]-(V_U-V_L)D_1-V_L=0 \\ F_2(X,D_1,D_2,E,k)=k\left\{V_{ref}-v_{exv}[\Phi_3\Phi_2\Phi_1 x_n+(\Phi_3\Phi_2\Psi_1+\Phi_3\Psi_2+\Psi_3)E]\right\} \\ -(V_U-V_L)D_2-V_L=0 \end{cases} \quad (2.41)$$

The system comprises of three transcendental equations, as D_1 and D_2 appear both as linearly and as exponential terms within the transition matrices. To solve this system, a Matlab™ [54] routine was developed. The process for evaluating the bifurcation parameter is illustrated in the flowchart shown in Figure 2.86.

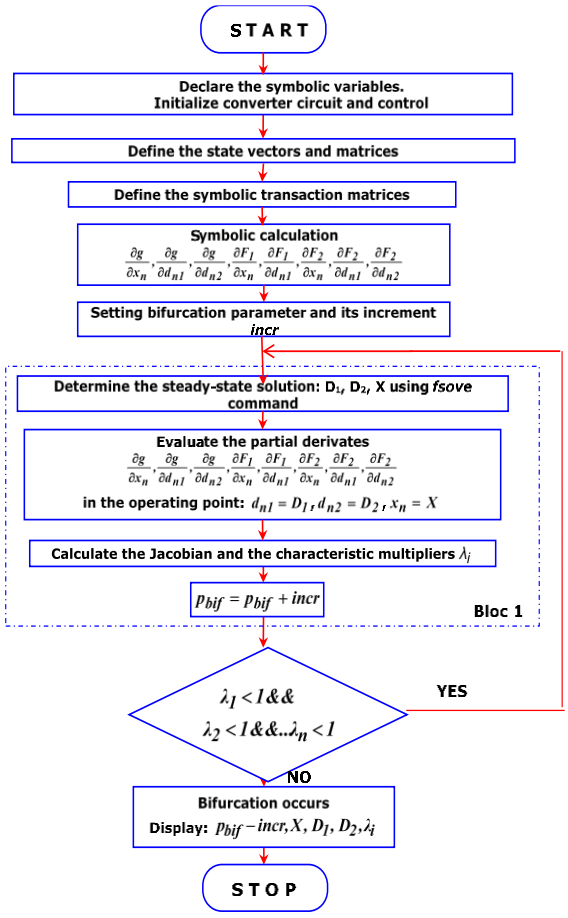

Figure 2.86 The flowchart used to evaluate the value of the parameter when bifurcation occurs.

Simulations results

The parameters of the two-phase boost converter under investigation are as follows: $E = 6V;\ L_1 = 400\mu H;\ L_2 = 1.6\mu H; C = 100\mu F;\ R = 10\Omega;\ T = 20\mu s; n = 2;\ V_U = 1V;\ V_L = 0V;\ V_{ref} = 18V.$

A Matlab™ [54] program was developed, based on the flowchart in Figure 2.86, to determine the parameter value at which bifurcation occurs. The bifurcation parameter selected was the controller gain *k*, and the results are summarized in Table 2.7.

Table 2.7 Characteristic multipliers of the two-phase boost converter for increasing values of the gain *k*.

k	*Eigenvalue*			*Absolute value*		*Comment*
	λ_1	λ_2	λ_3	$abs(\lambda_1)= abs(\lambda_2)$	$abs(\lambda_3)$	
0.0400	0.9955+0.0375i	0.9955-,0375i	0.9999	0.9962	0.9999	stable
0.0450	0.9966+ 0.0384i	0.9966-0,0384i	0.9999	0.9973	0.9999	stable
0.0500	0.9978+0.0392i	0.9978-0,0392i	0.9999	0.9974	0.9999	stable
0.0550	0.9990+0.0400i	0.9990-0.0400i	0.9999	0.9998	0.9999	stable
0.0557	0.9991+0.0401i	0.9991-0.0401i	0.9999	1.0000	0.9999	bifurcation
0.0600	1.0002+0.0408i	1.0002-0.0408i	0.9999	1.0010	0.9999	bifurcation
0.0700	1.0028+0.0423i	1.0028-0.0423i	0.9999	1.0037	0.9999	bifurcation
0.0800	1.0054+0.0437i	1.0054-0.0437i	0.9999	1.0063	0.9999	bifurcation

The analysis reveals that one characteristic multiplier remains real, positive, and less than unity, approaching the unity circle as the gain increases. The other two multipliers are complex conjugates, exceeding unity in magnitude when k=0.0557, marking the bifurcation point. This behaviour corresponds to a Neimark-Sacker bifurcation [66], [67] - [68], characterized by one real multiplier within the unity circle and two complex multipliers leaving it.

To validate the theoretical considerations, the same converter was simulated using the Caspoc™ package [50], as shown in Figure 2.87.

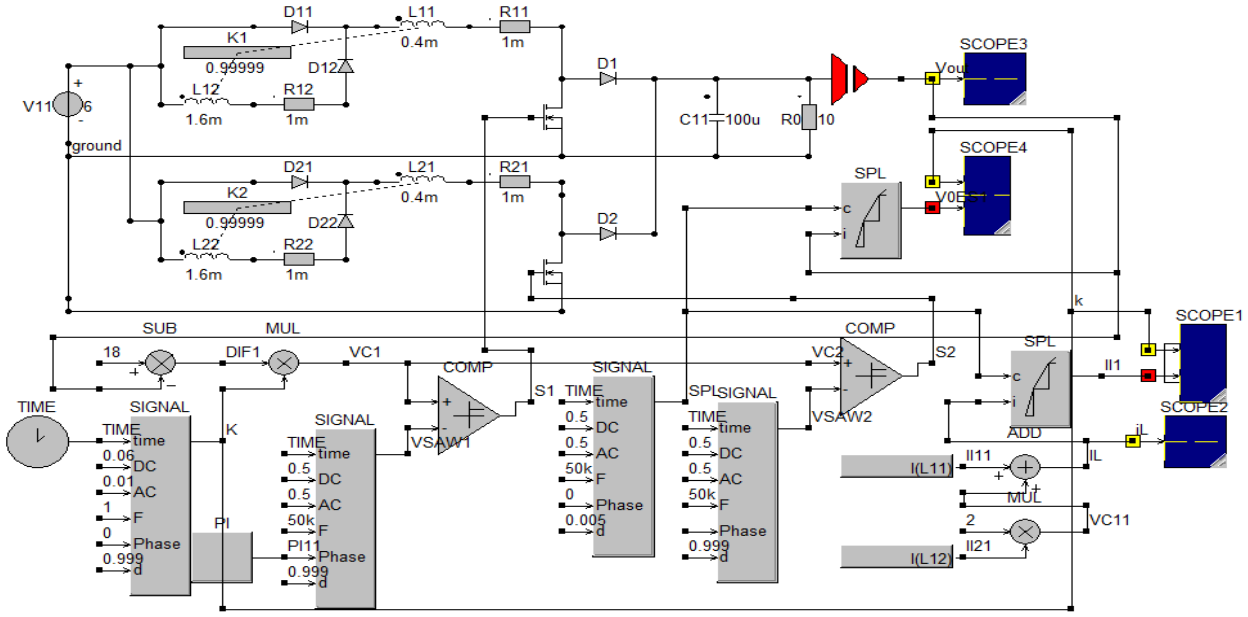

Figure 2.87 Caspoc™ schematic for two phase Boost converter.

The simulation slowly increased the gain k from 0.05 to 0.06 over one second to achieve a sequence of quasi-steady states without significant transients. Figure 2.88 demonstrates stable operation at k=0.05, consistent with Table 2.7.

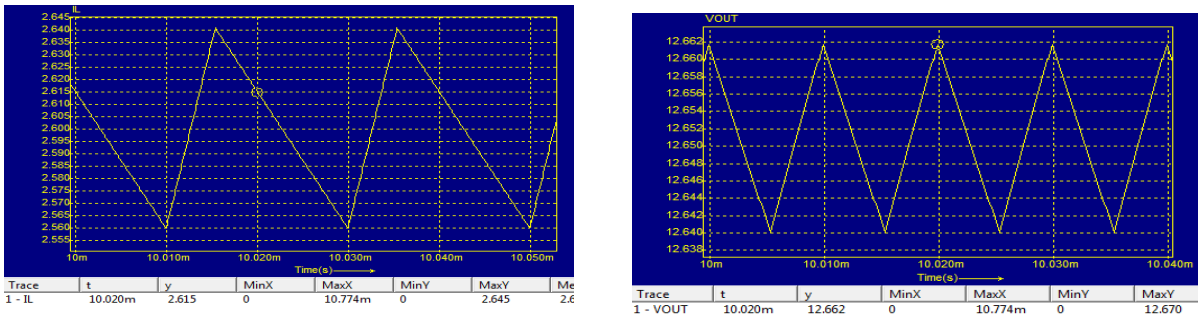

Figure 2.88 Stable operation of the converter for k=0.05. Inductor current – left; Output voltage – right.

The bifurcation diagram in Figure 2.89-left reveals the bifurcation at k=0.055631, closely matching the theoretical value of k=0.0557 derived in Matlab™, with an excellent relative error of 0.12%. Finally, Figure 2.89 right, illustrates the converter behaviour for k=0.06, where unstable

operation is evident due to the presence of a 450.45 Hz subharmonic. These simulation results closely complained with the theoretical predictions, providing strong validation.

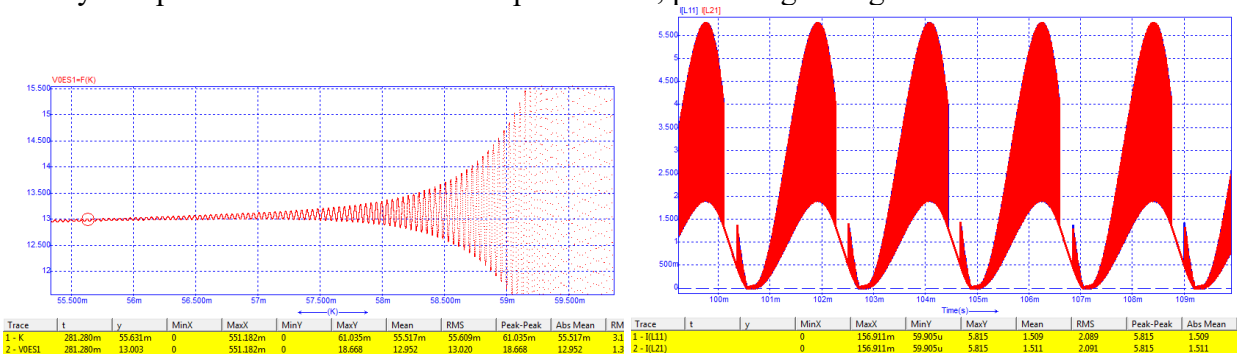

Figure 2.89 Bifurcation diagram – left; Subharmonic when k=0.06 – right.

Conclusions

An exact stability analysis of a two-phase Boost converter, derived from a classical hybrid single-phase Boost topology with coupled inductors [11], was presented, [17]. The study develops a discrete linearized model, calculates the characteristic multipliers using a Matlab™ routine, and validates the results through Caspoc™ simulations. The methodology is adaptable to other types of two-phase converters, with future research focusing on multiphase topologies involving simultaneous transistor conduction.

2.1.2.2 Bifurcation study in DCM operated DC-DC switching converters

A new mathematical technique for analysing DC-DC converters operating in *DCM* is proposed in [37]. This method overcomes the limitations of classical techniques like averaging and Taylor expansion, which can lead to inaccuracies. The new approach involves exact calculations of the state transition matrices and the Jacobian, providing higher accuracy and general applicability to any DC-DC *DCM* converter with any control type. The method allows for an exact iterative map derivation and precise calculation of operating points, providing exact values for parameters leading to bifurcation. This method is highly general and can be applied to any DC-DC converter with any control technique without modifying the analysis algorithm. It can chose any bifurcation parameter, such as controller gain k, input voltage V_g, or load resistance R. The algorithm can be easily implemented in Matlab™ or similar programs. The method validity is confirmed by theoretical, simulations, and experimental results, with an error margin of less than 0.94%.

State description of the discontinuous conduction mode

Discontinuous Conduction Mode occurs when at least one switching event is asynchronous to the control signals, primarily governed by the diode passive switching behaviour. The switching period T consists of three topological states: the on-state (d_nT), when the transistor conducts; the off-state (h_nT), when the transistor is *off* and the diode is forward biased; and the third state ($(1-d_n-h_n)T$), when both semiconductors are *off*.

DCM differs from *CCM* due to the introduction of this third state, Figure 2.90. State-space modelling is used to describe the system, where each topological state corresponds to a Linear Time-Invariant (LTI) circuit, making the converter piecewise linear. Discrete variables are denoted

with subscripts (e.g., $z_n=z(nT)$), while continuous variables at specific moments use rounded brackets (e.g., $z(nT+d_nT)$). These mathematical tools enable precise analysis of *DCM*-operated DC-DC converters.

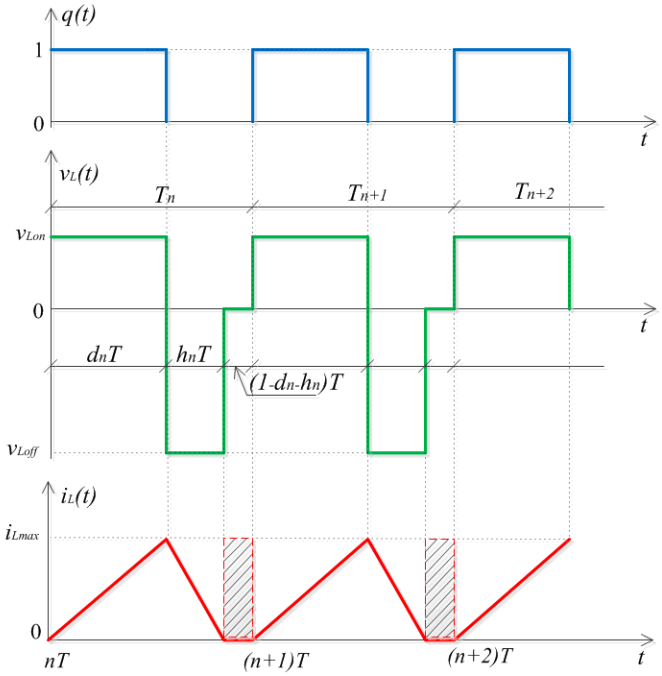

Figure 2.90 Transistor switching function, inductor voltage and inductor current in *DCM* operated dc-dc converters.

The LTI equations governing the operation of a *DCM*-operated DC-DC converter vary across the three topological states. They can be expressed as follows:

$$\begin{cases} \frac{dx}{dt} = A_1 x + B_1 u(t) \ when \ t \in [nT, \ (n+d_n)T) \\ \frac{dx}{dt} = A_2 x + B_2 u(t) \ when \ t \in [\ (n+d_n)T, \ (n+d_n+h_n)T) \\ \frac{dx}{dt} = A_3 x + B_3 u(t) \ when \ \ t \in [\ (n+d_n+h_n)T, \ (n+1)T) \end{cases} \quad (2.42)$$

Here, $x(t)$ represents the state vector, $u(t)$ is the input vector, and A_i, B_i (where i=1,2,3) are the state-space matrices corresponding to each switching state. These equations describe the piecewise linear dynamics of the *DCM* mode in switching converters.
Under these conditions, the operation of the converter can be described using the discrete state equation:

$$x_{n+1} = \varphi_3\varphi_2\varphi_1 \cdot x_n + (\varphi_3\varphi_2\psi_1 + \varphi_3\psi_2 + \psi_3) \cdot u_n \quad (2.43)$$

Where, x_n is the state vector at the beginning of the switching period, Φ_i represent the state transition matrices for each topological state (i=1,2,3), Ψ_i represent the input effect matrices for each state and u_n is the input vector, that includes the supply voltage and other constant voltage or current sources resulted from the device models.

The transition matrices involved in (2.43) are:

$$\begin{cases} \varphi_1 = e^{A_1 d_n T} \quad ; \quad \psi_1 = e^{A_1 d_n T} \cdot \left(\int_0^{d_n T} e^{-A_1 \tau} d\tau \right) \cdot B_1 \\ \varphi_2 = e^{A_2 h_n T} \quad ; \quad \psi_2 = e^{A_2 (d_n + h_n) T} \cdot \left(\int_{d_n T}^{(d_n + h_n) T} e^{-A_2 \tau} d\tau \right) \cdot B_2 \\ \varphi_3 = e^{A_3 (1 - d_n - h_n) T} \quad ; \quad \psi_3 = e^{A_3 T} \cdot \left(\int_{(d_n + h_n) T}^{T} e^{-A_3 \tau} d\tau \right) \cdot B_3 \end{cases} \quad (2.44)$$

When matrices A_i are nonsingular ψ_1, ψ_2, ψ_3 can be written in a simplified form as:

$$\begin{cases} \psi_1 = A_1^{-1} (\varphi_1 - I) B_1 \\ \psi_2 = A_2^{-1} (\varphi_2 - I) B_2 \\ \psi_3 = A_3^{-1} (\varphi_3 - I) B_3 \end{cases} \quad (2.45)$$

The steady-state solution of a *DCM*-operated DC-DC converter is periodic, meaning that the duty cycles d_n and h_n become constant, denoted as D and H, while the input vector u_n is also constant, represented as U.

The transition matrices Φ_1, Φ_2, Φ_3 and input effect matrices Ψ_1, Ψ_2, Ψ_3 are symbolically evaluated, ensuring an exact description of system dynamics. If B_i=0, then Ψ_i=0, which applies to boost converters. In any converter in which the transistor is in series to the supply voltage, matrices B_i are zero in all topological states when the transistor is *off*.

Thus the steady-state transition matrices take the form:

$$\begin{cases} \Phi_1 = e^{A_1 D T} \; ; \quad \Psi_1 = e^{A_1 D T} \left(\int_0^{D T} e^{-A_1 \tau} d\tau \right) \cdot B_1 \\ \Phi_2 = e^{A_2 H T} \; ; \quad \Psi_2 = e^{A_2 (D+H) T} \left(\int_{HT}^{(D+H) T} e^{-A_2 \tau} d\tau \right) \cdot B_2 \\ \Phi_3 = e^{A_3 (1 - D - H) T} \; ; \quad \Psi_3 = e^{A_3 T} \left(\int_{(D+H) T}^{T} e^{-A_3 \tau} d\tau \right) \cdot B_3 \end{cases} \quad (2.46)$$

Under these conditions, the steady-state constant state vector X can be determined by imposing the condition:

$$x_{n+1} = x_n = X \quad (2.47)$$

Substituting into the discrete state equation (2.43), the steady-state equation results in:

$$X = (I - \Phi_3 \Phi_2 \Phi_1)^{-1} \cdot (\Phi_3 \Phi_2 \Psi_1 + \Phi_3 \Psi_2 + \Psi_3) U \quad (2.48)$$

The new method for determining bifurcation parameter

In this thesis, only the final equations necessary for determining the bifurcation parameter are presented, providing a concise mathematical framework for stability analysis. The detailed derivation steps, including the formulation of the discrete state-space model, linearization process, and elimination of auxiliary variables, are thoroughly outlined in the full article. The methodology follows a systematic approach, ensuring that all relevant transformations and simplifications are rigorously justified.

The next equation represents the linearized small-signal model of the *DCM*-operated DC-DC converter, describing perturbations around the steady-state operating point. They are essential for computing the Jacobian matrix, which enables the analysis of system stability and bifurcation prediction through eigenvalues evaluation.

$$\begin{cases} \hat{x}_{n+1} = \left.\frac{\partial g}{\partial x_n}\right|_{OP} \hat{x}_n + \left.\frac{\partial g}{\partial d_n}\right|_{OP} \hat{d}_n + \left.\frac{\partial g}{\partial h_n}\right|_{OP} \hat{h}_n + \left.\frac{\partial g}{\partial u_n}\right|_{OP} \hat{u}_n \\ \left.\frac{\partial F_1}{\partial x_n}\right|_{OP} \hat{x}_n + \left.\frac{\partial F_1}{\partial d_n}\right|_{OP} \hat{d}_n + \left.\frac{\partial F_1}{\partial h_n}\right|_{OP} \hat{h}_n + \left.\frac{\partial F_1}{\partial u_n}\right|_{OP} \hat{u}_n = 0 \\ \left.\frac{\partial F_2}{\partial x_n}\right|_{OP} \hat{x}_n + \left.\frac{\partial F_2}{\partial d_n}\right|_{OP} \hat{d}_n + \left.\frac{\partial F_2}{\partial h_n}\right|_{OP} \hat{h}_n + + \left.\frac{\partial F_2}{\partial u_n}\right|_{OP} \hat{u}_n = 0 \end{cases} \quad (2.49)$$

In general, the symbol $\left.\frac{\partial z}{\partial r}\right|_{OP}$ denotes the partial derivative of the function z with respect to the variable r, evaluated in the steady-state operating point.

Since the linearized model in (2.49) is an *LTI* system, the last two equations allow for expressing the small-signal perturbations $\hat{d}_n$ and $\hat{h}_n$ in terms of the state perturbation $\hat{x}_n$ and input perturbation $\hat{u}_n$. Substituting these expressions into the first equation leads to the final proposed mathematical model, which fully characterizes the local stability behavior of the *DCM*-operated DC-DC converter.

$$\hat{x}_{n+1} = \left(\left.\frac{\partial g}{\partial x_n}\right|_{OP} + \left.\frac{\partial g}{\partial d_n}\right|_{OP} \left.\frac{\frac{\partial F_1}{\partial h_n}\frac{\partial F_2}{\partial x_n} - \frac{\partial F_1}{\partial x_n}\frac{\partial F_2}{\partial h_n}}{\frac{\partial F_1}{\partial d_n}\frac{\partial F_2}{\partial h_n} - \frac{\partial F_1}{\partial h_n}\frac{\partial F_2}{\partial d_n}}\right|_{OP} + \left.\frac{\partial g}{\partial h_n}\right|_{OP} \left.\frac{\frac{\partial F_1}{\partial x_n}\frac{\partial F_2}{\partial d_n} - \frac{\partial F_1}{\partial d_n}\frac{\partial F_2}{\partial x_n}}{\frac{\partial F_1}{\partial d_n}\frac{\partial F_2}{\partial h_n} - \frac{\partial F_1}{\partial h_n}\frac{\partial F_2}{\partial d_n}}\right|_{OP} \right) \hat{x}_n + \quad (2.50)$$

$$+ \left(\left.\frac{\partial g}{\partial u_n}\right|_{OP} + \left.\frac{\partial g}{\partial d_n}\right|_{OP} \left.\frac{\frac{\partial F_1}{\partial h_n}\frac{\partial F_2}{\partial u_n} - \frac{\partial F_1}{\partial u_n}\frac{\partial F_2}{\partial h_n}}{\frac{\partial F_1}{\partial d_n}\frac{\partial F_2}{\partial h_n} - \frac{\partial F_1}{\partial h_n}\frac{\partial F_2}{\partial d_n}}\right|_{OP} + \left.\frac{\partial g}{\partial h_n}\right|_{OP} \left.\frac{\frac{\partial F_1}{\partial u_n}\frac{\partial F_2}{\partial d_n} - \frac{\partial F_1}{\partial d_n}\frac{\partial F_2}{\partial u_n}}{\frac{\partial F_1}{\partial d_n}\frac{\partial F_2}{\partial h_n} - \frac{\partial F_1}{\partial h_n}\frac{\partial F_2}{\partial d_n}}\right|_{OP} \right) \hat{u}_n$$

Jacobian J is easily identified as:

$$J = \left.\frac{\partial g}{\partial x_n}\right|_{OP} + \left.\frac{\partial g}{\partial d_n}\right|_{OP} \left.\frac{\frac{\partial F_1}{\partial h_n}\frac{\partial F_2}{\partial x_n} - \frac{\partial F_1}{\partial x_n}\frac{\partial F_2}{\partial h_n}}{\frac{\partial F_1}{\partial d_n}\frac{\partial F_2}{\partial h_n} - \frac{\partial F_1}{\partial h_n}\frac{\partial F_2}{\partial d_n}}\right|_{OP} + \left.\frac{\partial g}{\partial h_n}\right|_{OP} \left.\frac{\frac{\partial F_1}{\partial x_n}\frac{\partial F_2}{\partial d_n} - \frac{\partial F_1}{\partial d_n}\frac{\partial F_2}{\partial x_n}}{\frac{\partial F_1}{\partial d_n}\frac{\partial F_2}{\partial h_n} - \frac{\partial F_1}{\partial h_n}\frac{\partial F_2}{\partial d_n}}\right|_{OP} \quad (2.51)$$

Equation (2.51) reveals that in order to apply the bifurcation analysis, it is necessary to compute the partial derivatives of g, F_1 and F_2 with respect to the state vector x_n the duty cycle d_n, and h_n. Additionally, since the linearization process depends on evaluating these derivatives in the steady-state operating point, the exact steady-state solution must first be determined. To achieve this from equation (2.52) the steady-state duty cycle D is first determined followed by the computation of H using (2.53), once D is known. Finally, the steady-state state vector X is obtained from (2.48) These three equations, (2.52), (2.53), and (2.48), represent together a nonlinear system that must be numerically solved to determine the steady-state solution $\{D, H, X\}$, given a known input vector U.

$$-D + k\left[V_{ref} - V_{exv} \cdot (\Phi_1 X + \Psi_1 U)\right] = 0 \quad (2.52)$$

$$V_{exi}\ [\Phi_2\Phi_1 X + (\Phi_2\Psi_1 + \Psi_2)U] = 0 \quad (2.53)$$

$$X = (I - \Phi_3\Phi_2\Phi_1)^{-1} \cdot (\Phi_3\Phi_2\Psi_1 + \Phi_3\Psi_2 + \Psi_3)U \quad (2.54)$$

Bifurcation analysis using the proposed mathematical model

A Matlab-based bifurcation analysis was performed on a boost DC-DC converter using proportional voltage-mode control presented in Figure 2.91, with the amplifier gain k chosen as the bifurcation parameter. The study demonstrated that at k=1.1589, a negative characteristic multiplier exits the unit circle, indicating a period-doubling bifurcation [69], [70], [71] which was confirmed through simulations and experiments. Additionally, similar analysis was carried on

higher-order converters (SEPIC, Zeta), showing excellent agreement between theory, simulations, and experimental results.

Converter parameters are the following: V_g=16V; V_{ref}=22V; C=220µF; T=333.33µs; R=78Ω; L=1209µH; transistor on resistance R_{on}=0.2Ω; and diode forward voltage is V_D=0.4V; sawtooth parameters are V_U=3.5V; V_L=0.7V.

For the boost converter under study, the state vector is chosen as: $x = [i_L \ v_C]^t$ and $u = [V_g \ V_D]^t$. The state matrices are:

$$A_1 = \begin{bmatrix} -\frac{R_{on}}{L} & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}; \quad A_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}; \quad A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \qquad (2.55)$$

$$B_1 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix}; \quad B_2 = \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} \\ 0 & 0 \end{bmatrix}; \quad B_3 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}; \qquad (2.56)$$

where, i_L represents the inductor current, v_C represents the capacitor voltage and V_g is the input voltage.

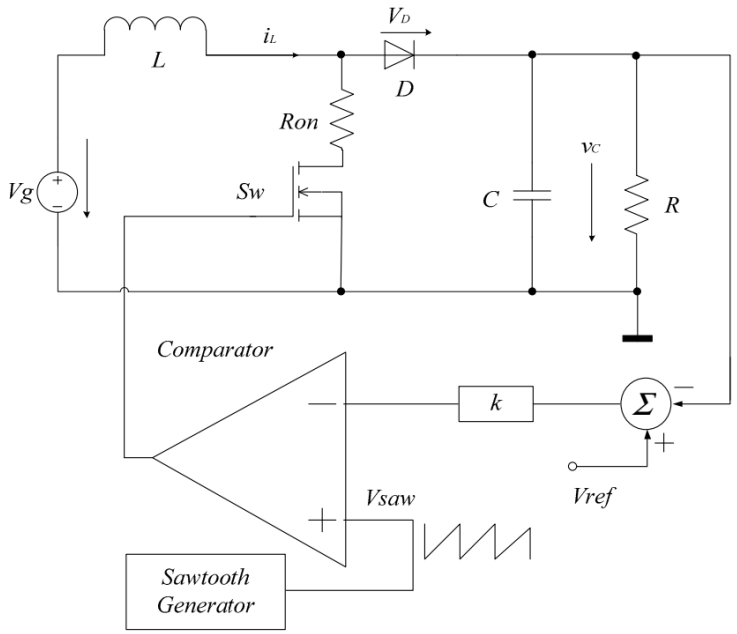

Figure 2.91 Proportional voltage-mode controlled boost converter.

The Matlab™-based bifurcation analysis was performed using the programs presented in the appendix of the paper [37]. The program flow chart is presented in Figure 2.92. The study found that at k=1.1589, a negative characteristic multiplier exits the unit circle, indicating a period-doubling bifurcation, with results confirmed with an accuracy of 0.01%. This phenomenon, inherent to DCM operation, will be further validated through circuit simulations and experimental results. The evolution of the characteristic multipliers values as the bifurcation parameter k is progressively increased is presented in Table 2.8. The bold value denotes the threshold when bifurcation occurs.

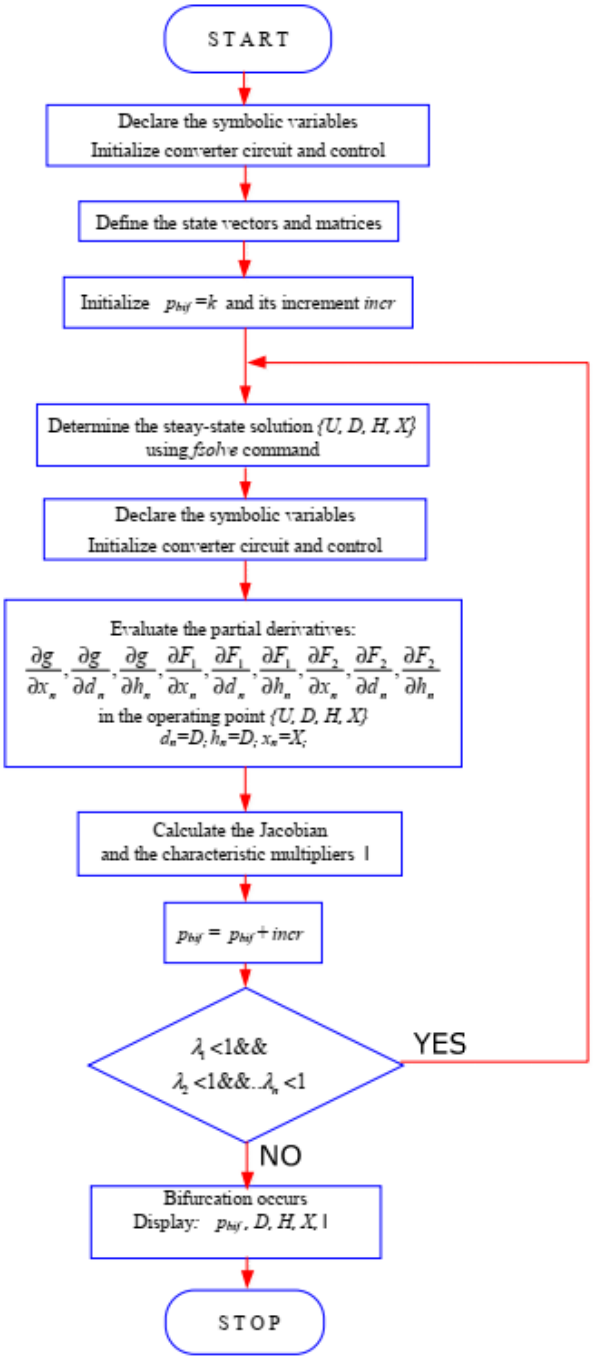

Figure 2.92 Flowchart of the Matlab program for determining the critical bifurcation parameter value.

Table 2.8 Characteristic multipliers of the boost converter for increasing values of the gain k.

Gain k	Eigenvalue l_1	Eigenvalue l_2	Remarks
1.1560	-0.9945	0.0000	stable
1.1570	-0.9964	0.0000	stable
1.1580	-0.9983	0.0000	stable
1.1589	**-1.0000**	**0.0000**	**Bifurcation**
1.1600	-1.0020	0.0000	Bifurcation
1.2000	-1.0775	0.0000	Bifurcation
1.3000	-1.2715	0.0000	Bifurcation

A Caspoc™ circuit simulation was performed to validate the theory, Figure 2.93, where the bifurcation parameter k was slowly varied from 1.1 to 1.2 over 1 second to ensure quasi-steady-state operation. The resulting bifurcation diagram, obtained in SCOPE3, plots k on the x-axis and sampled output voltage on the y-axis to analyse stability.

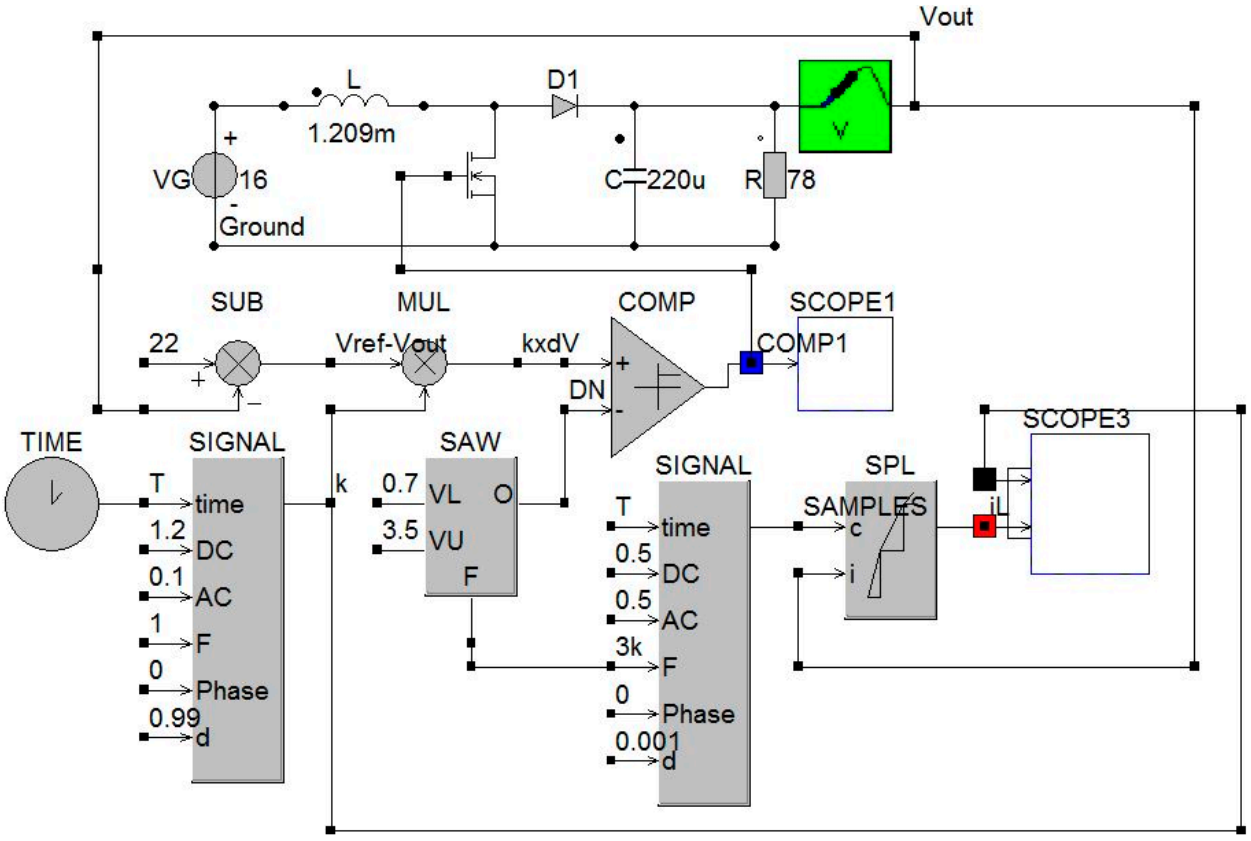

Figure 2.93 Caspoc™ schematic for the proportional voltage-mode controlled boost converter.

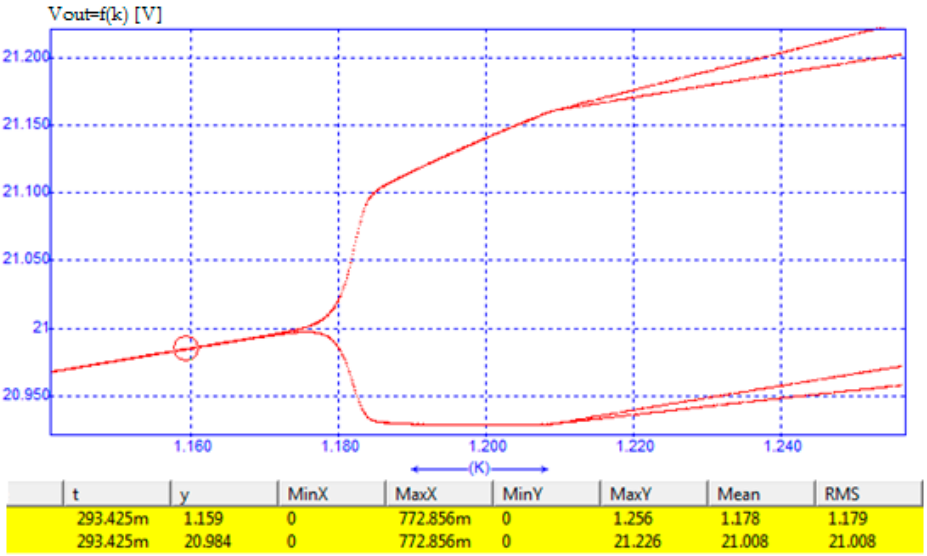

Figure 2.94 The simulated bifurcation diagram of the boost DCM converter employing proportional voltage-mode control.

Figure 2.95, confirms that the first period-doubling bifurcation occurs at k=1.159, closely matching the Matlab™ prediction of k=1.1589 with a 0.092% relative error, while Figure 2.96 a and Figure 2.96 b confirm stable operation at k=1.1, while Figure 2.96 c shows the inductor current waveform at k=1.2, exceeding the bifurcation threshold and aligning with the bifurcation diagram period-doubling prognosis, as further validated by the phase portrait in Figure 2.96 d.

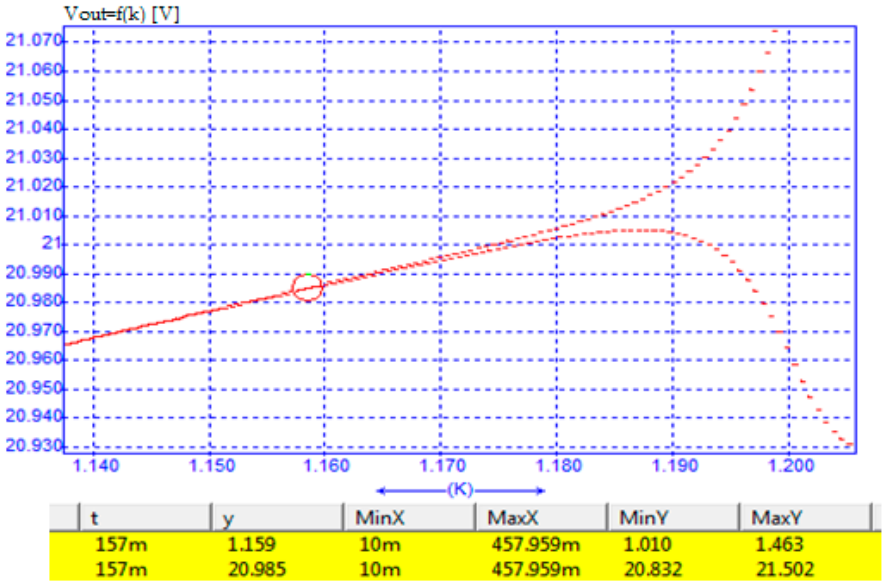

Figure 2.95 Magnified image around the bifurcation point. Clearly bifurcation appears at k = 1.159.

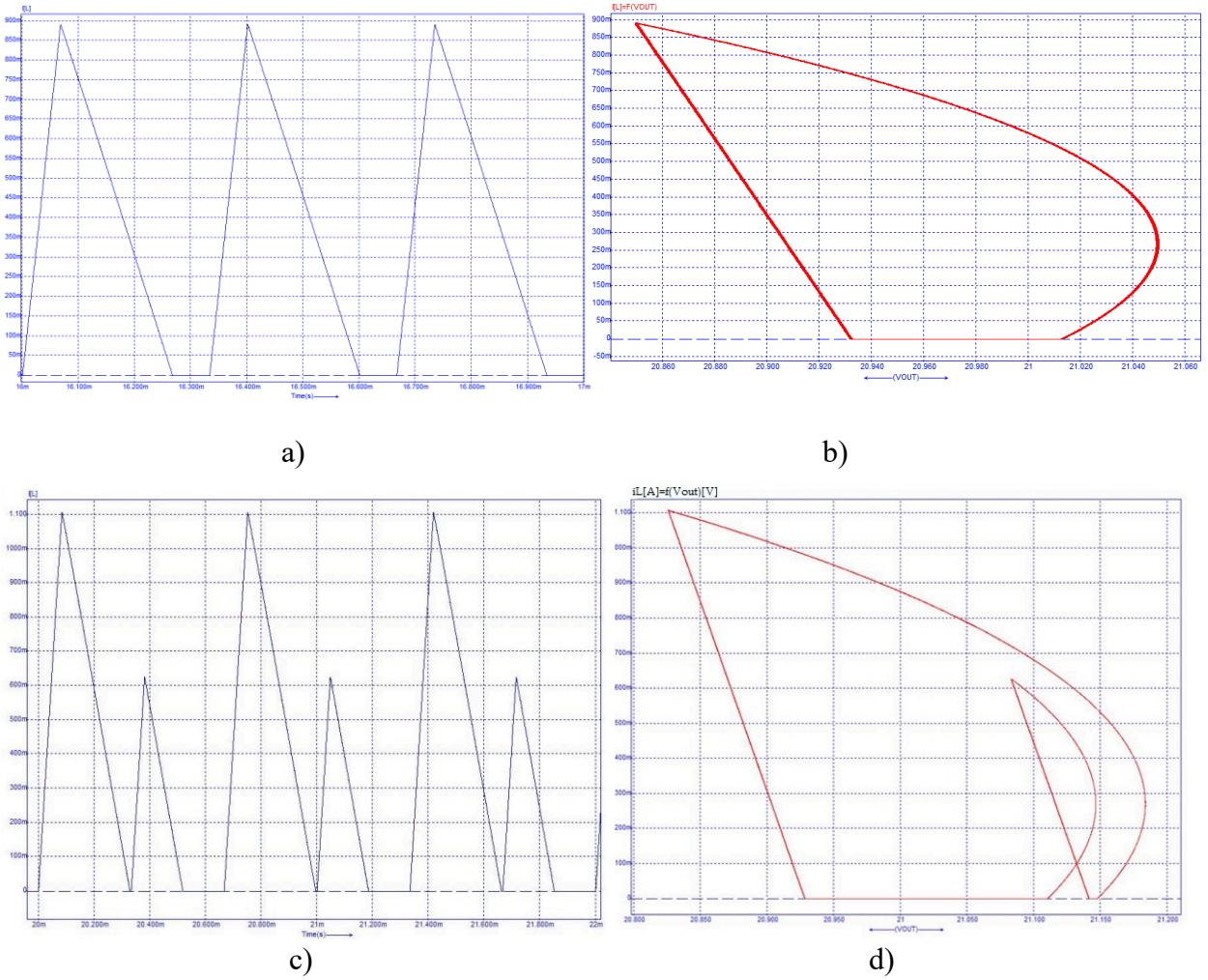

Figure 2.96 (a) The inductor current waveform for k = 1.1. The horizontal dotted line denotes the zero level and the solid line the inductor current. (b) phase portrait for stable operation, k = 1.1. (c) Inductor current for parameter k = 1.2, higher than bifurcation threshold value of 1.1589. Unstable operation with period doubling (period 2 subharmonic) is obvious and (d) - phase portrait for k = 1.2, higher than 1.1589, confirming period doubling.

As k increases beyond the first bifurcation (e.g., at k=1.215), a period-4 bifurcation occurs, which can be numerically determined by computing the Jacobian of $f \circ f$ using the same approach as period-2 bifurcation, and with further increase in k, the system eventually transitions into chaotic behaviour.

The experimental setup schematic is shown in Figure 2.97, where the differential amplifier, composed of *IC1* and resistors R_1 to R_4, determines the gain k, ensuring also that the typical condition of the differential amplifier is satisfied.

$$R_2 \cdot (R_{1p} + R_{11}) = R_4 \cdot (R_{3p} + R_{31}) \quad (2.57)$$

$$k = \frac{R_2}{R_{11}+R_{1p}} = \frac{R_4}{R_{31}+R_{3p}} \quad (2.58)$$

The experimental setup allows for gain k adjustment between 1.08 and 2.16 using the resistors in the differential amplifier, while the sawtooth waveform across capacitor C and potentiometer P_2 determine the SG3524 circuit operating frequency of 3 kHz. The SG3524 outputs, connected in parallel, generate short set pulses for the flip-flop, with pulse width

controlled by potentiometer P_1, and *IC2* amplifying the pulses to ensure proper threshold crossing. The reset signal is provided by comparator *IC3*, ensuring correct switching operation.

For k=1.08, Figure 2.98 (left) shows experimentally obtained waveforms, confirming stable operation as predicted by both Matlab™ [54] and Caspoc™ [50] simulations, with the inductor current exhibiting the typical *DCM* waveform shape. Additionally, the phase portrait in Figure 2.98 (right) further validates the stable steady-state operation of the system.

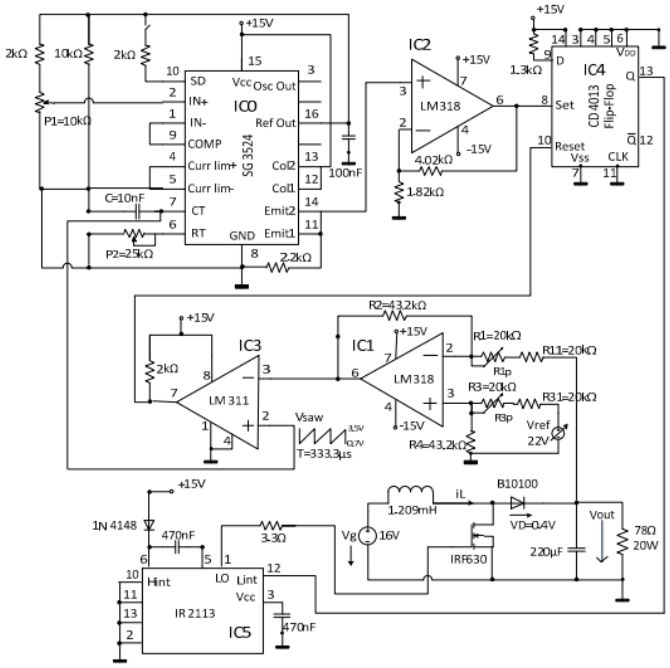

Figure 2.97 Schematic of the experimental boost DCM converter employing proportional voltage-mode control.

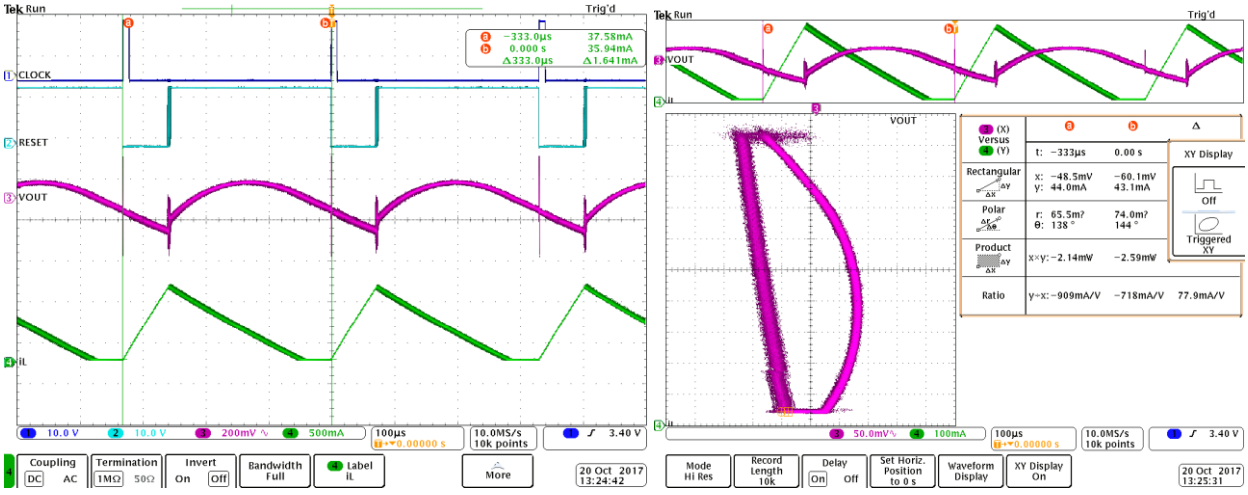

Figure 2.98 Set signal and reset signals of IC4. Stable operation can be remarked. Inductor current and output voltage waveform (this up to down order) for k = 1.08 – left; Phase portrait for k = 1.08 – right.

The gain factor k is then progressively increased while monitoring the inductor current, and bifurcation is identified when two consecutive switching periods exhibit different peak values, with the corresponding bifurcation threshold recorded. Figure 2.99 shows the transition from stable operation to bifurcation, where the inductor current peaks begin to differ, indicating the onset of period-doubling. The experimental bifurcation threshold is found at k=1.17, closely matching the Matlab™ [54] and Caspoc™ [50] predictions of k=1.16, with a relative error of only 0.94%. The minor discrepancy arises from device non-idealities such as R_{on}, V_D variations, neglected series resistance in passive components, and measurement uncertainties. Yet, the results strongly validate the theoretical bifurcation analysis method.

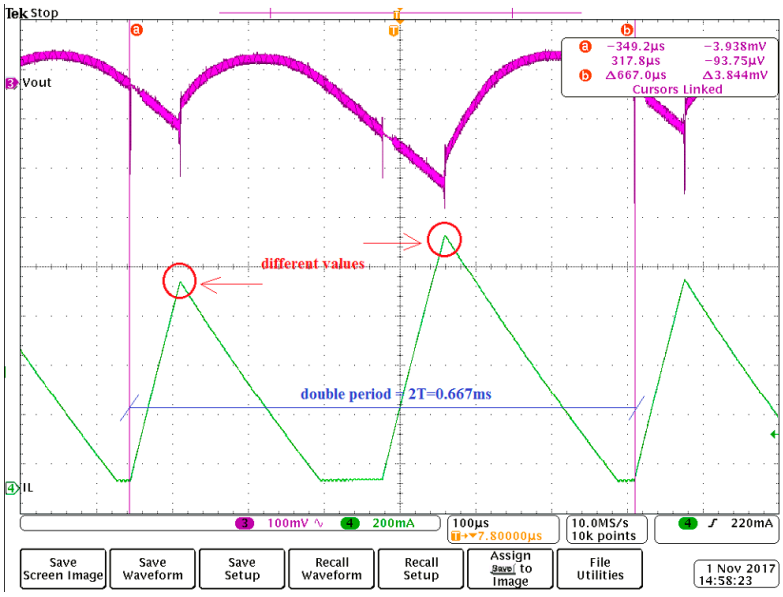

Figure 2.99 Inductor current and output voltage waveforms for k = 1.17. Notice that the peak inductor current values start to slightly differ in two consecutive periods and the period of the inductor current doubles compared to stable operation.

Further increasing the gain k reveals a more pronounced bifurcation, as shown in Figure 2.100 (left), where the inductor current and output voltage are displayed for k=1.20. At this point, the system exhibits a period-2 subharmonic oscillation, where the period of oscillation is half of the switching period, confirming the occurrence of period-doubling bifurcation. The corresponding phase portrait in Figure 2.100 (right) further validates this behaviour, displaying the typical trajectory of a period-2 bifurcation system.

A higher gain value eventually drives the converter into chaos, as shown in Figure 2.101, where both the waveforms and the phase portrait exhibit irregular, non-repetitive behaviour, confirming the system transition to chaotic operation.

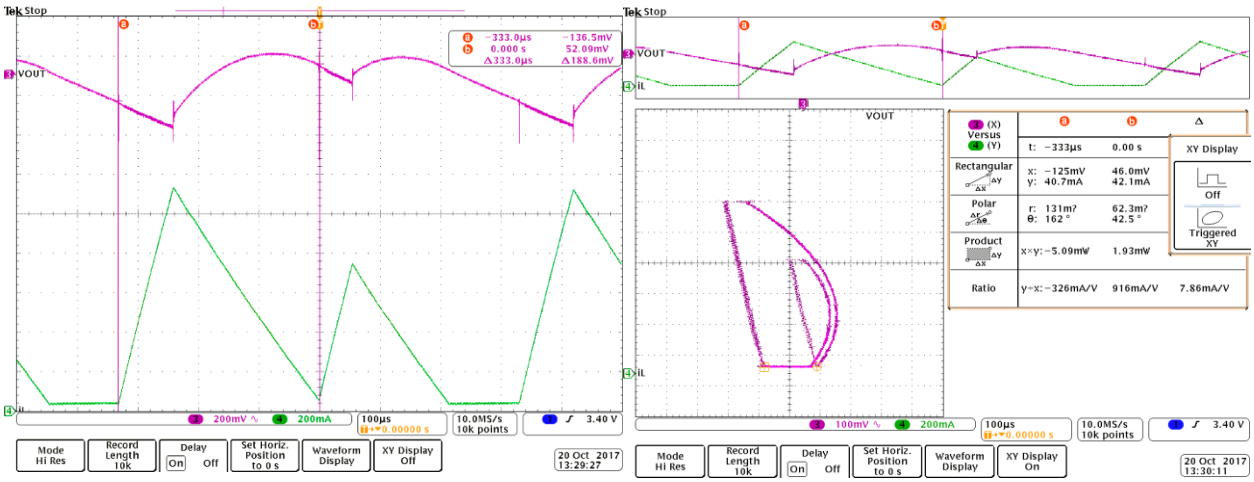

Figure 2.100 Inductor current and output voltage waveforms for k = 1.20. Bifurcation with period 2 operation is evident (left), phase portrait for k = 1.20, clearly revealing period 2 operation (right).

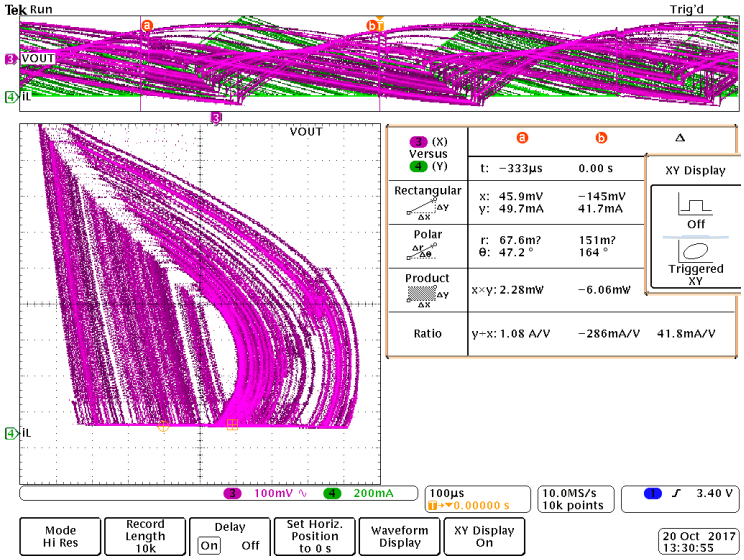

Figure 2.101 Chaotic operation of the converter corresponding to k = 1.50.

Input voltage as a bifurcation parameter

To further validate the proposed method, a bifurcation analysis was conducted using the input voltage V_g as the bifurcation parameter, while keeping the gain k constant at 1. Table 2.9 presents the characteristic multipliers as V_g gradually increases, showing that bifurcation occurs at V_g=17.125V. The Caspoc simulation predicts a bifurcation threshold of 17.045V, as depicted in Figure 2.102, with a relative error of 0.46%, confirming strong agreement between simulation and theory. The bifurcation phenomenon was further verified using Caspoc [50] simulations and experimentally confirmed, as shown in Figure 2.103, where the waveforms and phase portrait at V_g=16.5V indicate stable operation before reaching the bifurcation threshold.

Table 2.9 Characteristic multipliers of the boost converter for increasing values of the voltage V_g.

Voltage V_g	Eigenvalue l_1	Eigenvalue l_2	Remarks
16.6000	-0.8623	0.0000	stable
16.8000	-0.8983	0.0000	stable
17.0000	-0.9751	0.0000	stable
17.1250	**-1.0000**	**0.0000**	**Bifurcation**
17.2000	-1.0138	0.0000	Bifurcation
17.4000	-1.0572	0.0000	Bifurcation
17.6000	-1.1040	0.0000	Bifurcation

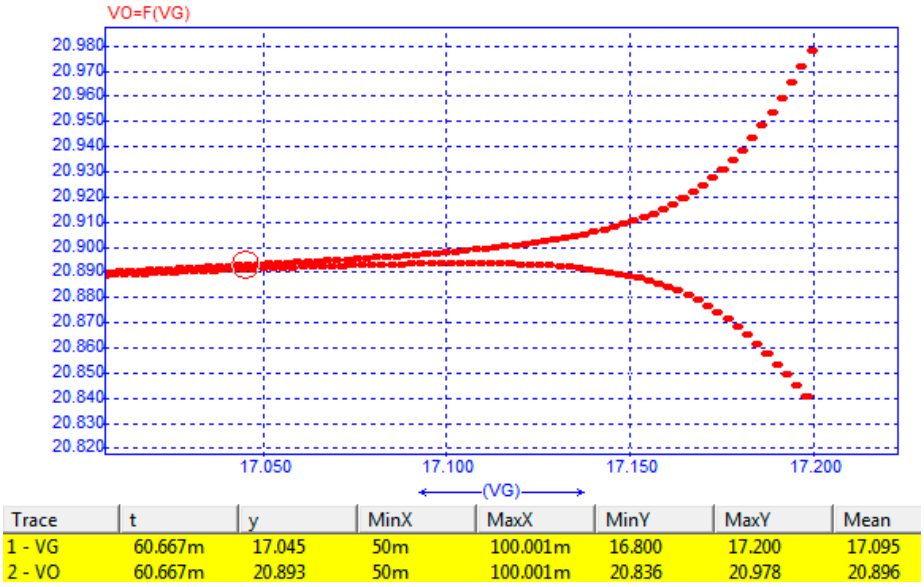

Figure 2.102 The simulated bifurcation diagram of the boost DCM converter: V_{out} = f(V_g).

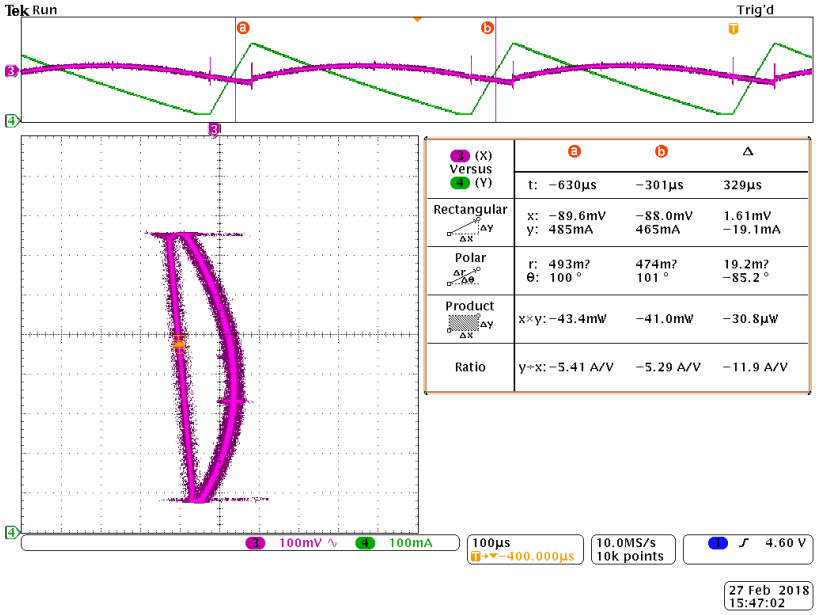

Figure 2.103 Phase portrait for V_g = 16.50 V, confirming stable operation.

Figure 2.104 illustrates the system behaviour at an input voltage of 17.2V, which exceeds the bifurcation threshold, clearly demonstrating the bifurcation phenomenon. Further increasing the input voltage pushes the system into chaotic operation, as shown in Figure 2.105.

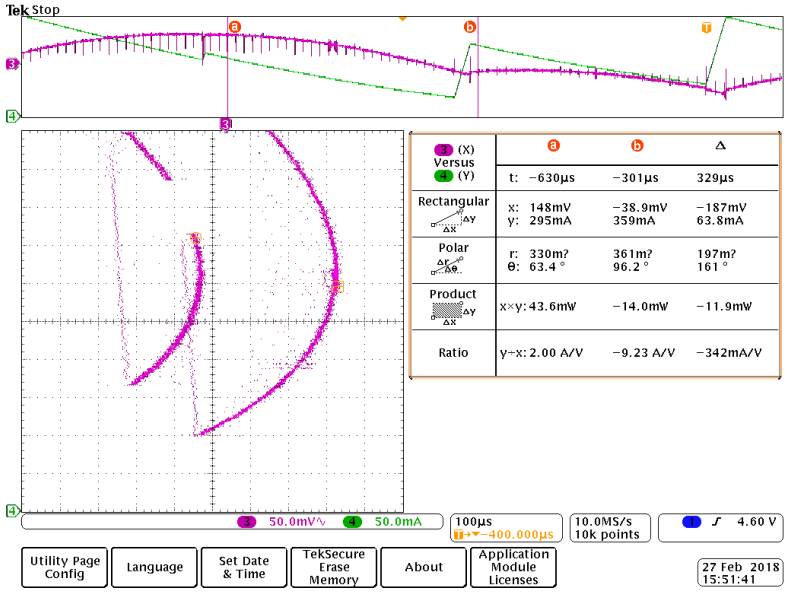

Figure 2.104 Phase portrait for V_g = 17.20 V, clearly revealing period 2 operation.

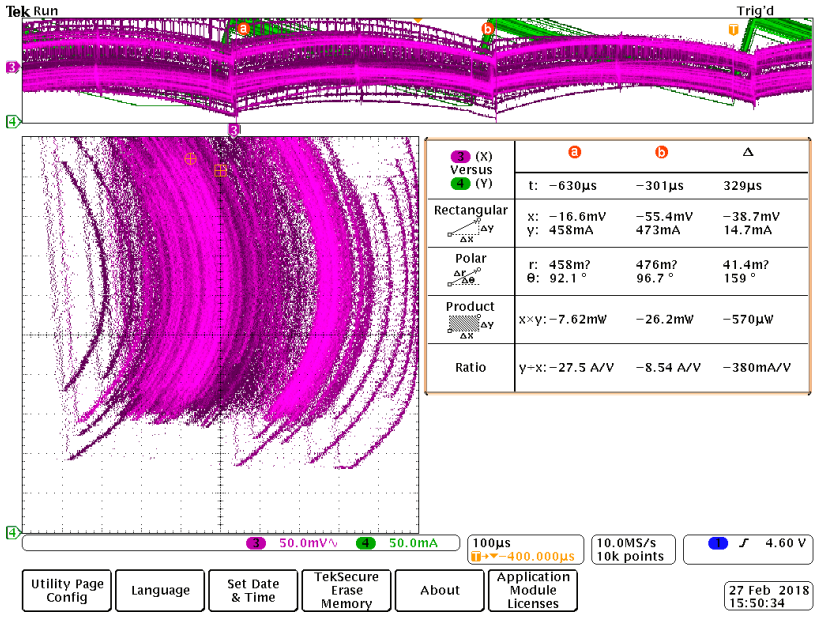

Figure 2.105 Chaotic operation of the converter corresponding to Vg = 17.80 V.

To conclude, in this paper [37], a new mathematical method for analysing and predicting bifurcation behaviour in *DCM*-operated DC-DC converters was proposed, offering exact calculations, without truncating state matrices, unlike most existing approaches that approximate waveforms as piecewise linear. This generalized method applies to any converter topology and control strategy, requiring only modifications of the state-space matrices and a constraint equation.

The algorithm is easily implementable in any mathematical software capable of computing the matrix exponential, ensuring higher accuracy than previously reported methods.

Experimental validation confirms excellent agreement between theory and practice, demonstrating the method reliability. Additionally, this approach enables precise prediction of the boundary between *DCM* and *CCM*, facilitating exact border collision detection. Unlike existing methods, it is applicable to both uniform or natural sampling and other diverse control techniques, including *CCM* and discontinuous capacitor voltage mode (*DCVM*), making it a versatile and superior analytical tool.

2.1.2.3 Design process for an ideal fourth-order buck-boost converter

A novel fourth-order buck-boost converter featuring coupled inductors, one MOSFET transistor, three diodes, two capacitors, and a separate inductor is presented in [31]. This converter offers two degrees of freedom, resulting in a significantly higher output voltage for the same duty cycle compared to the classical design. Theoretical analysis, simulations, and practical open loop experiments confirm its functionality. A state-space model is developed to derive the control-to-output transfer function, which is approximated by a second-order function (99.34% accuracy) for simplified controller design, then verified through closed-loop simulations.

In this section, the primary focus is on the closed-loop operation. Detailed explanations and the advantages of the converter can be found in [31].

The novel fourth-order buck-boost converter is derived from a fourth-order boost topology presented in [23] and illustrated in Figure 2.106. The process to obtain the buck-boost converter involves replacing the semiconductors with single-pole single-throw (SPST) switches, in order to identify the switching cell. Using the basic cell rotation concept, the switch synthesis is then performed [53], leading to the new topology shown in Figure 2.107. The coupled inductors L_2 and L_3 are modelled by an ideal transformer (*IT*) with a magnetizing inductor L_M, assuming a transformer ratio *n* higher than unity. The equivalent schematic, presented in Figure 2.108, includes the supply voltage V_g, transistor Q_1, diodes D_2, D_3, D_4, the coupled inductors L_2 and L_3, the stand-alone inductor L_1, the inner capacitor C_1, the output capacitor C_0 and the load R. The transistor operates at a switching frequency f_s with a switching period T_S, controlled via a *PWM* signal with duty cycle *D*.

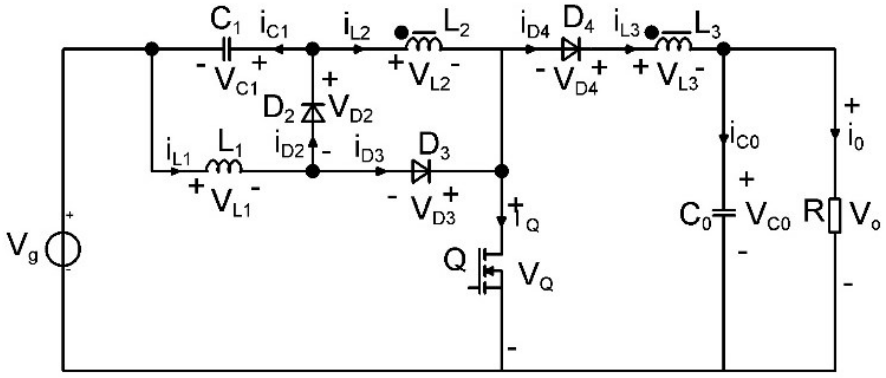

Figure 2.106 Boost converter from [23].

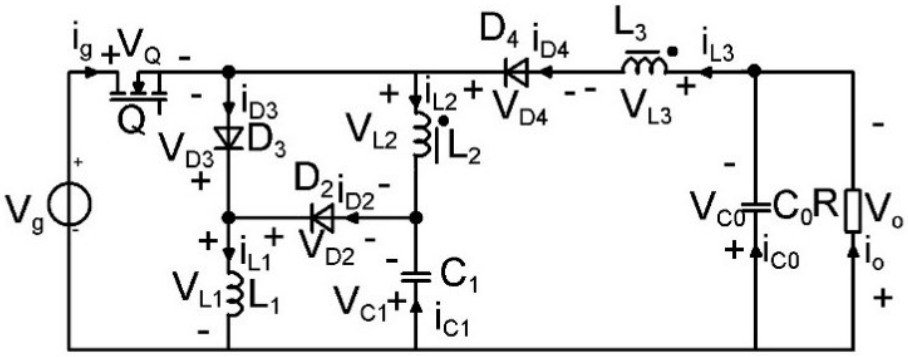

Figure 2.107 The proposed Buck-Boost converter with coupled inductors.

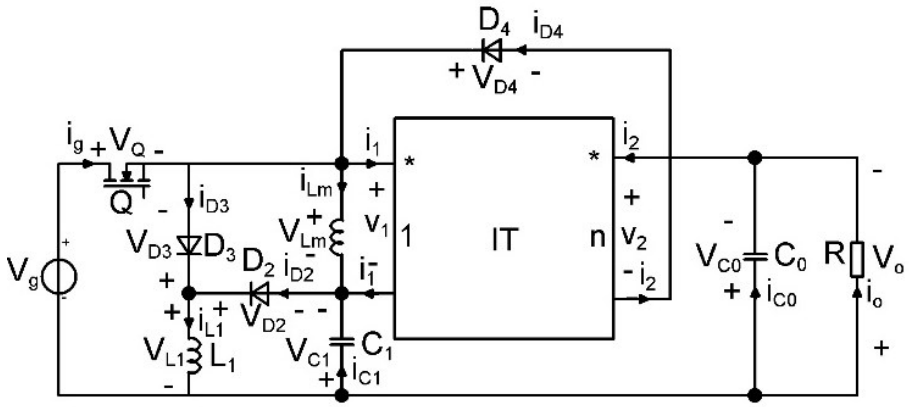

Figure 2.108 Equivalent schematic of the proposed Buck-Boost converter with coupled inductors.

The static conversion ratio of the converter is:

$$M = \frac{V_o}{V_g} = \frac{D\cdot(n+2-D)}{(1-D)^2} \qquad (2.59)$$

To determine the small-signal model of the proposed buck-boost converter, the state-space equations for each topological state were first derived. The state variables in vector $\boldsymbol{x}$ include the inductor currents (i_{L_1} and i_{L_M}) and the capacitor voltages (v_{C_1} and v_{C_0}). The input vector u consists solely of the supply voltage (v_g), while the output vector y is identical to the state vector [72]. By analysing the first and second topological state circuits, the derivatives of the state variables are expressed in terms of state and input variables. Subsequently, the corresponding matrices A_1, B_1, E_1 and F_1 for the first topological state are determined.

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_M} \\ 0 & 0 & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R\cdot C_0} \end{bmatrix};\ B_1 = \begin{bmatrix} \frac{1}{L_M} \\ \frac{1}{L_1} \\ 0 \\ 0 \end{bmatrix};\ E_1 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix};\ F_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}; \qquad (2.60)$$

For the second topological state, the matrices A_2, B_2, E_2 and F_2 are:

$$A_2 = \begin{bmatrix} 0 & 0 & \frac{1}{(n+1)\cdot L_M} & -\frac{1}{(n+1)\cdot L_M} \\ 0 & 0 & -\frac{1}{L_1} & 0 \\ -\frac{1}{(n+1)\cdot C_1} & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{(n+1)\cdot C_0} & 0 & 0 & -\frac{1}{R\cdot C_0} \end{bmatrix}; \; B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}; \; E_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; \; F_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}; \quad (2.61)$$

It is well established that, after applying averaging and linearization techniques, the control-to-output transfer function is expressed as in [72]:

$$G_c(s) = E_D \cdot (s \cdot I - A_D)^{-1} \xi_D + \zeta_D \quad (2.62)$$

where: $A_D = D \cdot A_1 + (1 - D) \cdot A_2$ etc,

$$X = -A_D^{-1} B_D U \quad (2.63)$$

$$\xi_D = (A_1 - A_2) \cdot X + (B_1 - B_2) \cdot U \quad (2.64)$$

$$\zeta_D = (E_1 - E_2) \cdot X + (F_1 - F_2) \cdot U \quad (2.65)$$

and I is the fourth order identity matrix.

Taking into consideration that the values of the converter are: input voltage: V_g = *15-20V*; output voltage: V_o = *120V*; output power: P_o = *20W*; switching frequency: f_s = *100 kHz* and transformer ratio: n=*1.5*. Using the MATLAB [54] program for calculation the output resistor is R=720Ω, the magnetizing inductor L_{Mmin}=L_{2min}=791.63µH and L_{3min}=$n^2 \cdot L_{2min}$=1.8mH. The inner inductor it is L_{1min}=219.90µH. In practice the value of L_1 was 271.93µH, L_2=811.6µH and L_3=1.975mH, resulting an n=1.56. The inner and output capacitors are equal to 10µF.

Applying the above formulae, the numerical control-to-output transfer function of proposed converter is, [72]:

$$G_C(s) = 970.1 \cdot \frac{-133e{-}15 \cdot s^3 + 77.75e{-}10 \cdot s^2 - 37.19e{-}6 \cdot s + 1}{3e{-}15 \cdot s^4 + 35.6e{-}14 \cdot s^3 + 44.19e{-}8 \cdot s^2 + 57.12 \cdot e{-}6 \cdot s + 1} \quad (2.66)$$

Since the control-to-output transfer function is of fourth order, the complexity of the controller design significantly increases. To address this, the fourth-order transfer function is approximated by a second-order function, enabling a simplified controller design. The approximation is valid up to half of the switching frequency, which represents the applicable range for the averaged model. Using the *tfest* command in MATLAB [54] the approximated control-to-output transfer function is obtained as:

$$G_{c\_aprox} = \frac{-8.292 \cdot 10^4 \cdot s + 2.221 \cdot 10^9}{s^2 + 131.1 \cdot s + 2.295 \cdot 10^6} \quad (2.67)$$

Figure 2.109, illustrates both the original and the approximated control-to-output transfer functions, demonstrating a high level of accuracy. The estimation data fit between the two functions is 99.34%, confirming the effectiveness of the approximation.

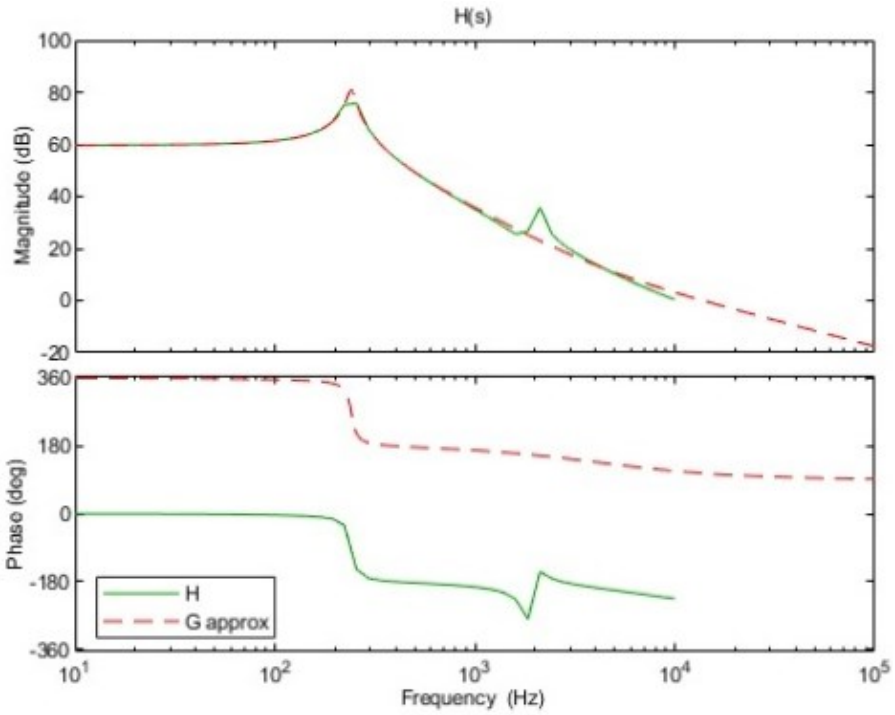

Figure 2.109 Control-to-output original transfer function (green), approximated control-to-output transfer function, red

The transfer function of the ideal type III error amplifier is [72]:

$$H_{AE}(s) = \frac{1}{\frac{s}{\omega_{UGF}}} \cdot \frac{(1+\frac{s}{\omega_{z1}})\cdot(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})\cdot(1+\frac{s}{\omega_{p2}})} \quad (2.68)$$

Using the pole placement method [72], the parameters of the error amplifier are determined as follows:

$$\omega_{ugf}=25.9703\ rad/s \quad (2.69)$$

$$\omega_{p1} = \omega_{ZESR}=26785.23\ rad/s \quad (2.70)$$

$$\omega_{p2}=3.1416e{+}05\ rad/s \quad (2.71)$$

$$\omega_{z1} = \omega_{z2} = \omega_0=1514.96\ rad/s \quad (2.72)$$

The closed-loop simulation results are presented in Figure 2.110, illustrating the system response to step changes in input voltage: 20V → 15V → 25V → 20V. The results show that the *DC* output voltage remains regulated at the desired -120V, with minimal overshoot and short transient response times, confirming the system stability and effectiveness. Additionally, Figure 2.111 displays the output of the error amplifier, exhibiting similar characteristics and further validating the control strategy.

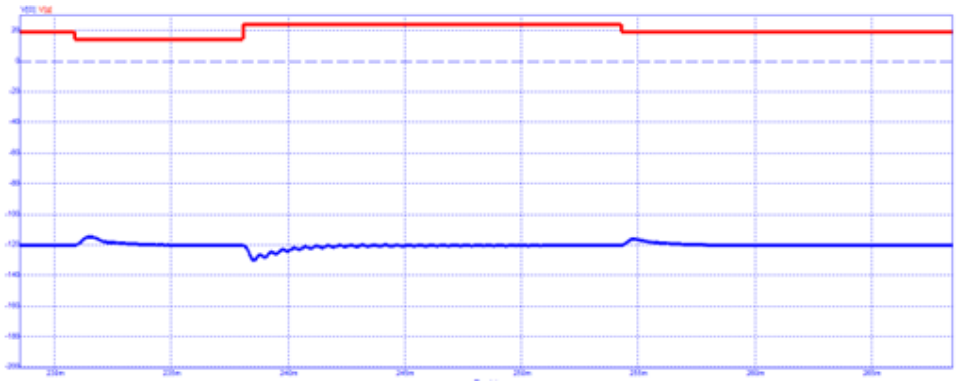

Figure 2.110 Dynamic behaviour at step changes in the input voltage: Input voltage (red-V_g), output voltage (blue-V_o).

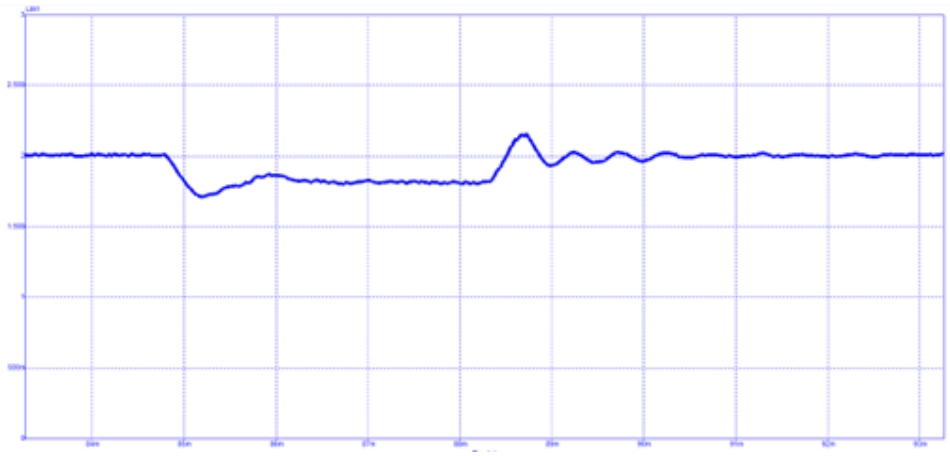

Figure 2.111 Controller output voltage.

The closed-loop analysis confirms the stability and effectiveness of the proposed controller, ensuring precise output voltage regulation with minimal overshoot and fast transient response.

2.1.2.4 Design process of a controller for a fourth-order quadratic buck converter with losses

The design process of a controller for a fourth-order quadratic buck converter with losses, emphasizing the importance of state-space modelling for small-signal analysis is also presented in [35]. Due to the complexity of a fourth-order system, the control-to-output transfer function is approximated to a second order using the *tfest* function, simplifying controller design. A Type III error amplifier plays a crucial role in achieving stability and improving system response. The proposed design is validated through simulations, focusing on the step response to input voltage and output resistance changes. The study confirms that reducing the system order maintains control performance, making it applicable to similar high-order converters.

The converter is derived from the fourth-order boost topology presented in [23] and illustrated in Figure 2.106. The process to obtain the buck topology is the same as for the buck-boost converter from [31], this architecture being part of the same family. The schematic of the buck converter is presented in Figure 2.112, and the equivalent model in Figure 2.113.

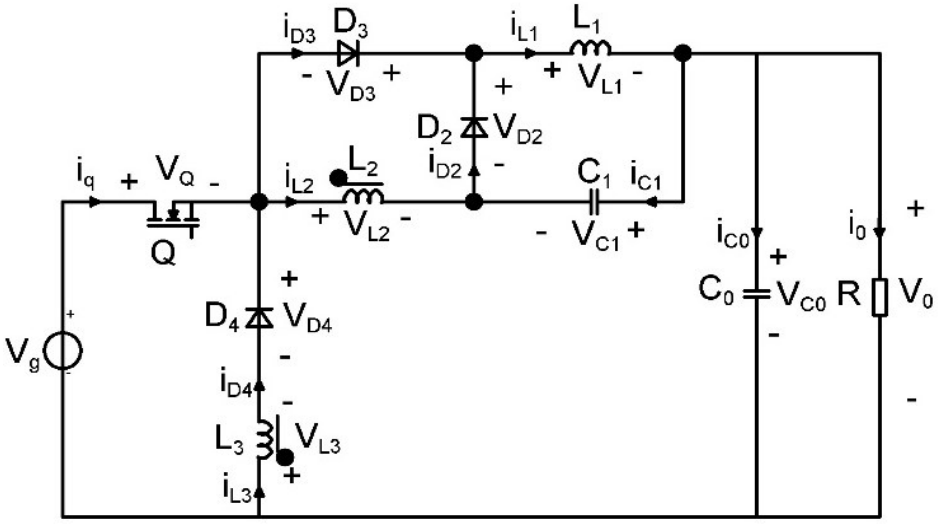

Figure 2.112 The proposed Buck-type topology with coupled inductors proposed in [35].

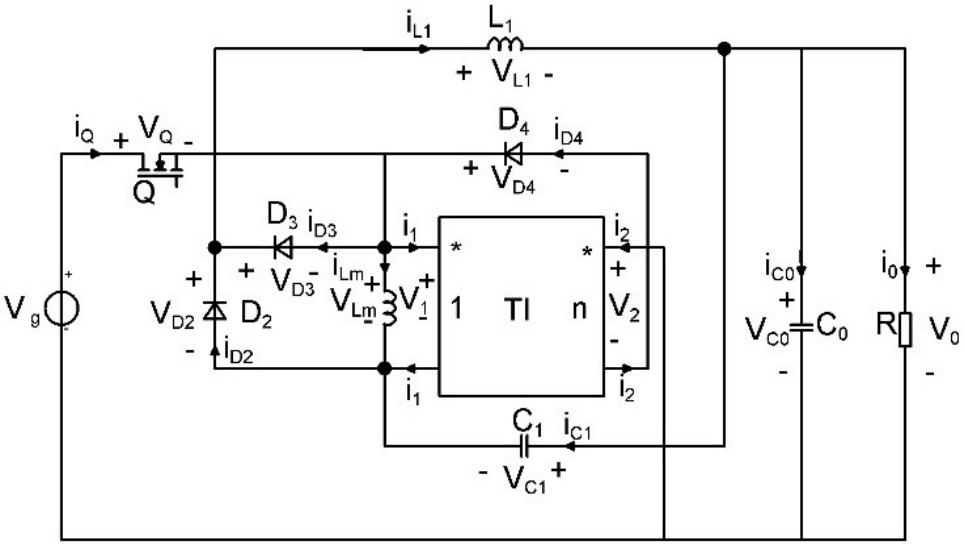

Figure 2.113 Equivalent model of the proposed Buck-type topology with coupled inductors.

The corresponding states of the converter can be seen in Table 2.10.

Table 2.10 Corresponding states of the converter.

Semiconductor devices	State 1	State 2
Q	On	Off
D_2	Off	On
D_3	On	Off
D_4	Off	On

The static conversion ratio, *M* is:

$$M = \frac{V_o}{V_g} = \frac{D \cdot (n+2-D)}{1+n \cdot D} \quad (2.73)$$

The step-down converter proposed is designed according to the following specifications:

- Input voltage: $V_g = 30V$;
- Output voltage: $V_o = 18V$;
- Output power: $P_o = 10\text{-}15W$;
- Switching frequency: $f_s = 100\ kHz$;
- Transformer ratio: n=0.66.

The output resistor value is R=33Ω. The theoretical and the simulated values of magnetizing inductor, L_M, which is equal to the value of L_2, inductor L_3, as well for the single inductor L_1, inner capacitor C_1 and output capacitor C_0 are presented in the Table 2.11. The calculations performed in MATLAB provide the minimum values for the components; therefore, in the simulation, higher values were used.

Table 2.11 Theoretical and simulated values of reactive elements.

Component	Minimum theoretical values	Simulated values
Coupled inductor L_2	398.84µH	463µH
Coupled inductor L_3	173.73µH	207µH
Single inductor L_1	264.83µH	266µH
Inner capacitor C_1	3.07 µF	10µF
Output capacitor C_0	1.81µF	10µF

Figure 2.114 presents the schematic with lossy elements, ensuring a more realistic representation of the system. By incorporating these losses, the state-space equations are refined, enhancing the accuracy of the control-to-output transfer function. This approach allows for better controller design, leading to improved performance and stability in practical applications.

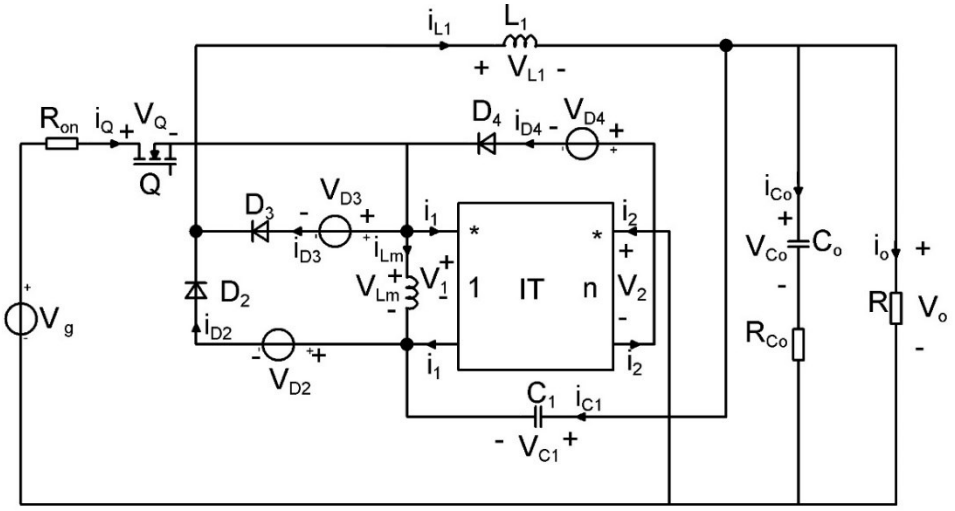

Figure 2.114 Equivalent model of the proposed Buck-type topology including losses.

To develop the small-signal model of the proposed buck-type converter, it is necessary to first establish the state-space equations corresponding to each topological state. The state variables, represented in vector x, include the inductor currents i_{L_1} and i_{L_M} and the capacitor voltages v_{C_1} and v_{C_o}. The input vector u comprises the supply voltage v_g and the forward voltage drops of the three diodes v_{D2}, v_{D3}, v_{D4}. The output vector y is identical to the state vector, ensuring consistency in

the system's representation. To streamline calculations, the notation R_{ech} is introduced, representing the equivalent parallel resistance at the converter output.
The matrices A_1, B_1, E_1 and F_1 corresponding to the first topological state are:

$$A_1 = \begin{bmatrix} -\frac{R_{on}+R_{ech}}{L_M} & -\frac{R_{on}+R_{ech}}{L_M} & \frac{1}{L_M} & -\frac{R}{L_M\cdot(R+R_{Co})} \\ -\frac{R_{on}+R_{ech}}{L_1} & -\frac{R_{on}+R_{ech}}{L_1} & 0 & -\frac{R}{L_M\cdot(R+R_{Co})} \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ \frac{R}{C_0\cdot(R+R_{Co})} & \frac{R}{C_0\cdot(R+R_{Co})} & 0 & -\frac{R}{C_0\cdot(R+R_{Co})} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L_M} & 0 & 0 & 0 \\ \frac{1}{L_1} & -\frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}; E_1 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; F_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}; \quad (2.74)$$

The matrices A_2, B_2, E_2 and F_2 corresponding to the second topological state will be derived as:

$$A_2 = \begin{bmatrix} -\frac{R_{ech}}{(1+n)^2\cdot L_M} & 0 & \frac{1}{(1+n)\cdot L_M} & -\frac{R}{L_M\cdot(R+R_{Co})\cdot(1+n)} \\ 0 & 0 & \frac{1}{L_1} & 0 \\ -\frac{1}{(1+n)\cdot C_1} & \frac{1}{C_1}0 & 0 & 0 \\ \frac{R}{C_0\cdot(R+R_{Co})} & \frac{R}{C_0\cdot(R+R_{Co})} & 0 & -\frac{R}{C_0\cdot(R+R_{Co})} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_M} \\ \frac{1}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}; E_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; F_2 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}; \quad (2.75)$$

After averaging and linearization, the control-to-output function results as follows:

$$G_c(s) = E_D \cdot (s \cdot I - A_D)^{-1}\xi_D + \zeta_D \quad (2.76)$$

Where: $A_D = D \cdot A_1 + (1-D)\cdot A_2$

$$X = -A_D^{-1}B_D U \quad (2.77)$$

$$\xi_D = (A_1 - A_2)\cdot X + (B_1 - B_2)\cdot U \quad (2.78)$$

$$\zeta_D = (E_1 - E_2)\cdot X + (F_1 - F_2)\cdot U \quad (2.79)$$

By applying the derived state-space equations, the numerical control-to-output transfer function of the proposed fourth-order quadratic buck converter is numerical calculated:

$$G_c(s) = \frac{2.173e258\cdot s^3 + 1.718e263\cdot s^2 + 5.747e266\cdot s + 5.165e271}{2.926e253\cdot s^4 + 9.228e256\cdot s^3 + 1.296e262\cdot s^2 + 2.733e265\cdot s + 1.237e270} \quad (2.80)$$

As expected, the control-to-output transfer function of the proposed fourth-order quadratic buck converter is initially expressed as a fourth-order function, introducing significant complexity in controller design. To address this challenge, a second-order approximation is employed, reducing the system complexity while maintaining accuracy within the valid frequency range (up to half of the switching frequency). The *tfest* function in MATLAB [54] is used to estimate a lower-order transfer function with two poles and two zeros, enabling a simplified yet effective controller design.

$$G_c(s) = \frac{-0.3247\, s^2 + 8.49e04 \cdot s + 5.707e09}{s^2 + 3063 \cdot s + 1.372e08} \quad (2.81)$$

Figure 2.115 presents a comparison between the original fourth-order transfer function and its second-order approximation, demonstrating the accuracy of the *tfest*-based estimation. The approximation achieves a data fit of 86.12%, indicating a high level of correlation between the two functions within the relevant frequency range.

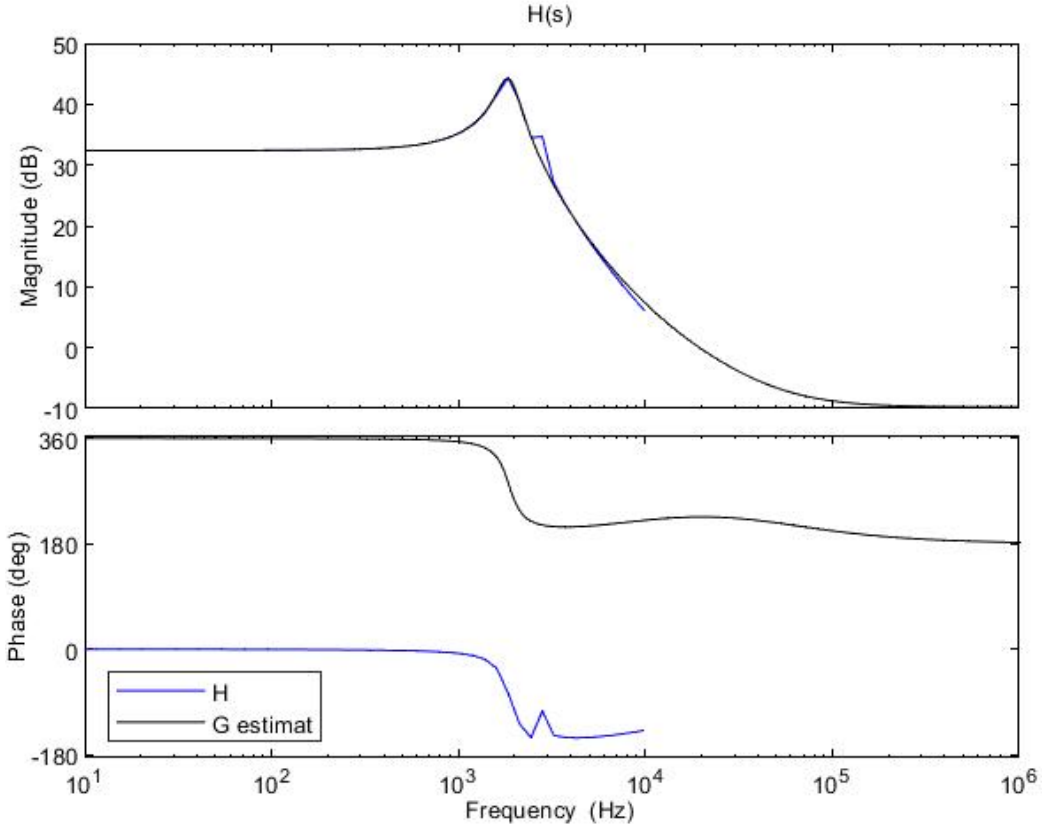

Figure 2.115 Initial control-to-output transfer function (blue) and approximated control-to-output transfer function (black).

The transfer function of the ideal type III error amplifier is [72]:

$$H_{AE}(s) = \frac{1}{\frac{s}{\omega_{UGF}}} \cdot \frac{(1+\frac{s}{\omega_{z1}})\cdot(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})\cdot(1+\frac{s}{\omega_{p2}})} \quad (2.82)$$

Using the pole-zero placement method described in reference [72], the specific parameters for the error amplifier are determined. A crossover frequency of 9 kHz is selected to optimize system

stability. To facilitate calculations, a MATLAB [54] script was developed, yielding the following results:

$$\omega_{ugf} = 5.4379e+03\ rad/s \quad (2.83)$$
$$\omega_{p1} = \omega_{ZESR} = 55455\ \text{rad/s} \quad (2.84)$$
$$\omega_{p2} = 3.1416e+05\ rad/s \quad (2.85)$$
$$\omega_{z1} = \omega_{z2} = \omega_0 = 11713\ rad/s \quad (2.86)$$

With these parameter values, the frequency response characteristics of the error amplifier are illustrated in Figure 2.116 (left), while the open-loop transfer function characteristics are shown in Figure 2.116 (right). Analysing Figure 2.116 (right), it is observed that the amplitude characteristic follows a monotonic decrease with a slope of -20 dB/decade, except for a peak caused by the high-quality factor in the denominator of (2.81). The actual crossover frequency is determined to be 7.3 kHz, with a phase margin of 20 degrees, ensuring system stability while maintaining responsiveness. The phase characteristic of *HAE3(s)* and the phase characteristic of *T(s)* are presented in Figure 2.117.

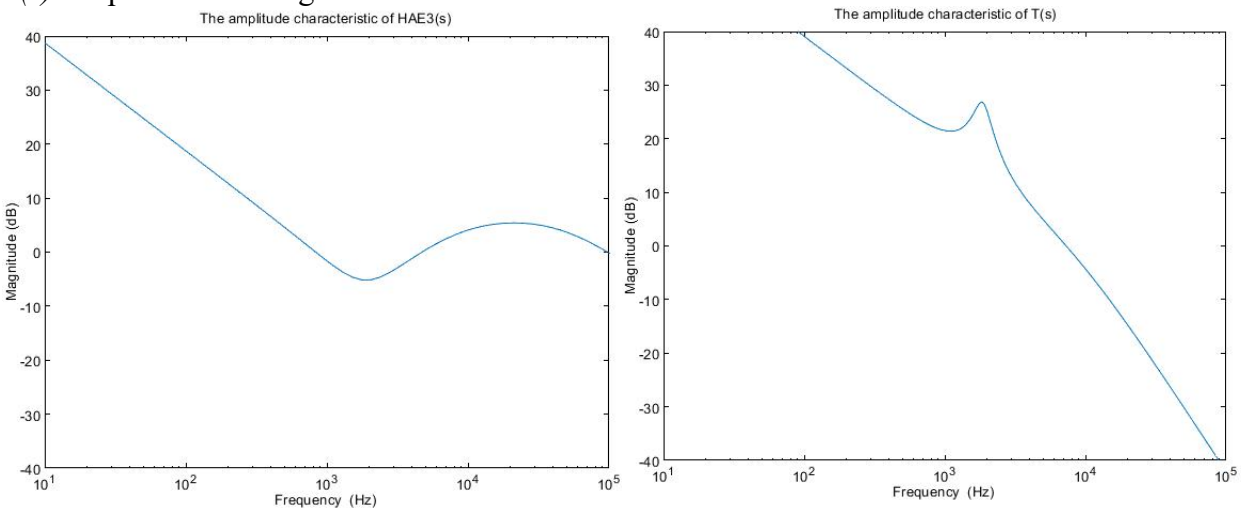

Figure 2.116 The amplitude characteristic of $H_{AE3}(s)$ -left, and the amplitude characteristic of *T(s)* -right.

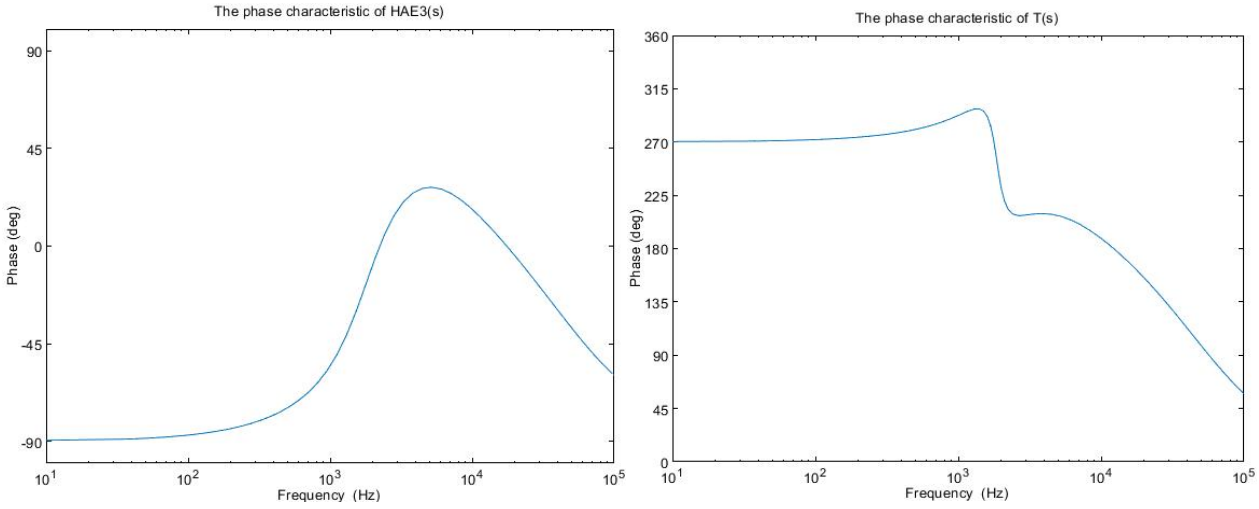

Figure 2.117 The phase characteristic of $H_{AE3}(s)$ – left, and the phase characteristic of *T(s)* – right.

The theoretical analysis is validated through CASPOC simulations, considering component losses and a 100 kHz switching frequency for the *PWM*-controlled transistor. The results show steady-state voltage regulation at 18V (Figure 2.118), diode voltage and current waveforms in different topological states (Figure 2.119 and Figure 2.120), and stable output voltage under step changes in input voltage (Figure 2.121) and load resistance variations (Figure 2.122). The output voltage remains well-regulated, with the load current exhibiting a quasi-rectangular waveform, though minor ringing effects occur due to the still low phase margin. Improving the transient response is possible by reducing the crossover frequency, for phase margin increase, at the expense of the longer response time.

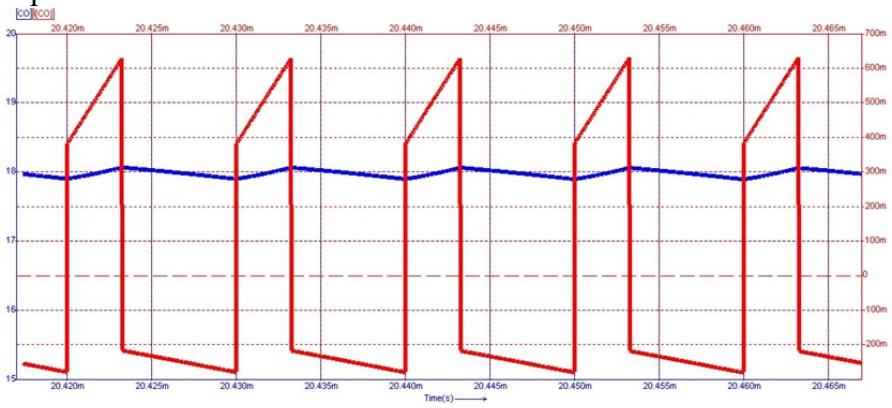

Figure 2.118 Voltage and current waveforms for the output capacitor C_0. Voltage regulation at 18V is observed.

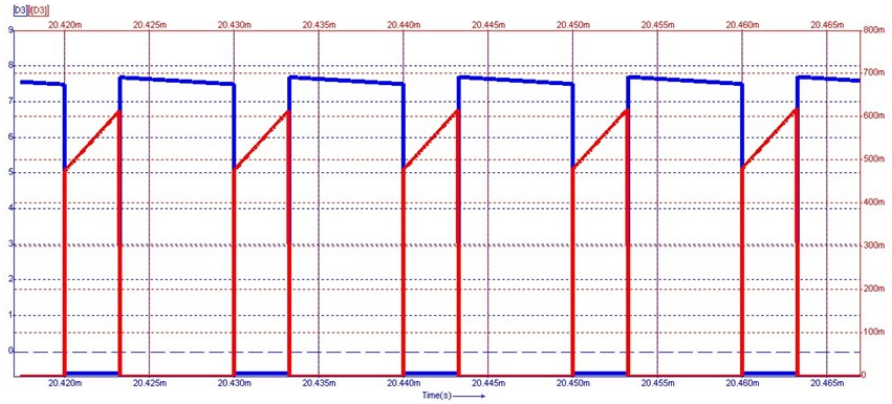

Figure 2.119 Voltage and current waveforms for diode D_3.

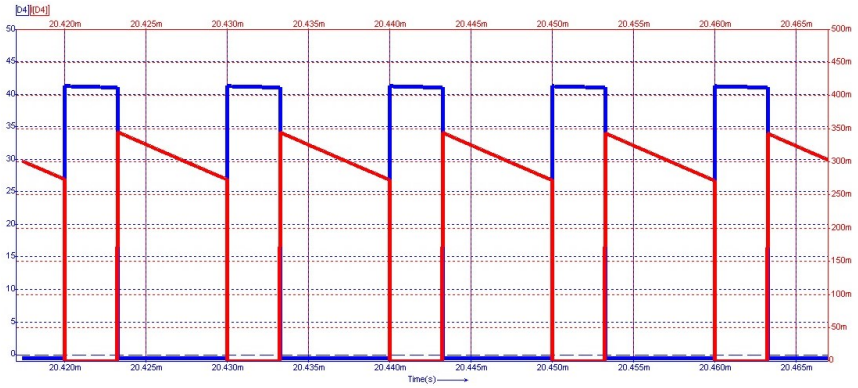

Figure 2.120 Voltage and current waveforms for diode D_4.

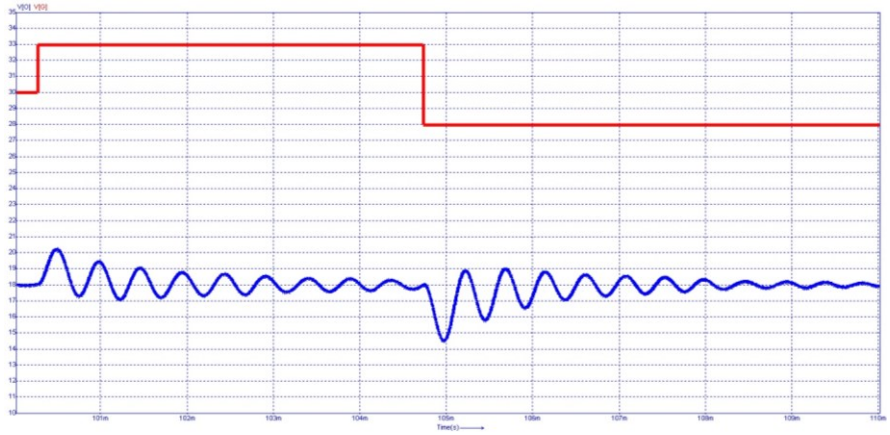

Figure 2.121 Dynamic behaviour for step changes in the input voltage: input voltage (red-V_g), output voltage (blue-V_O).

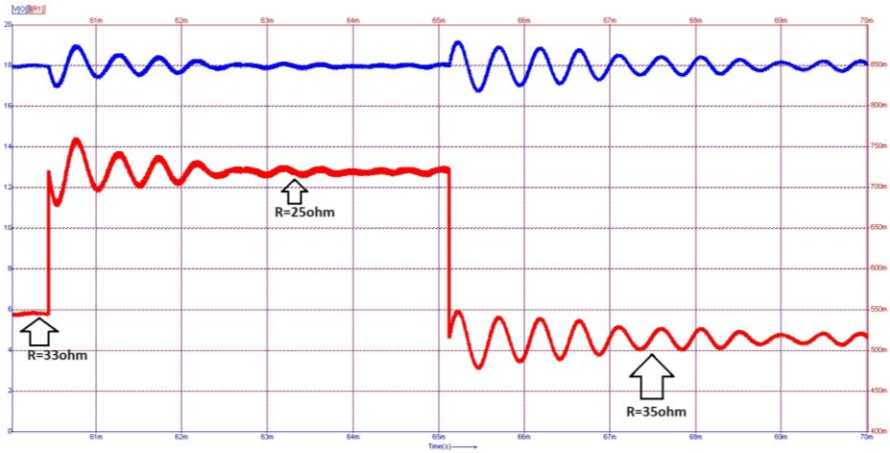

Figure 2.122 Dynamic behaviour for step changes in the load resistance: output voltage (blue-V_O), output current (red- I_{R1}).

The closed-loop operation, regulated with a Type III error amplifier, ensures fast transient response, effective voltage regulation, and system stability, even with an 86.12% approximation accuracy. The proposed converter design offers the advantage of a higher step-down ratio, improved efficiency, and good load regulation, making it suitable for applications requiring precise voltage control. This approach demonstrates that simplified controller design can effectively manage high-order converters, ensuring stable operation and reliable performance.

2.1.3 Photovoltaic applications

Renewable energy sources have gained significant attention due to their availability, environmental benefits, and applicability across diverse geographic locations and climates. Among these, electrical energy from renewable sources is particularly valued for its wide range of applications, easy transport, and independence from geographic constraints. Common production methods include photovoltaic (PV) panels, wind turbines, hydro turbines, and fuel cells, enabling local resource optimization while integrating into unified smart grids.

PV energy has seen exponential growth due to advancements in technology, offering improved efficiency, reduced costs, and scalability. It allows connection to public grids with the potential to sell excess energy. However, standalone or grid-connected PV systems face the issue of low output voltage from PV modules. This can be addressed by connecting modules in series or using step-up DC-DC converters, which are widely used in modern power conversion systems for their high voltage boost capabilities.

2.1.3.1 A new hybrid inductor-based Boost DC-DC converter suitable for photovoltaic systems

Inspired by [7] and published in [19], the converter introduced achieve a higher step-up conversion ratio than the classical converter. The operation principle, *DC* analysis, key equations, and theoretical waveforms are discussed, followed by *AC* analysis of inductor currents and capacitor voltage ripples and the *CCM* operation condition that was derived. Considering the conduction losses, the static conversion ratio of the converter, as well as the small-signal control-to-output transfer function and the audiosusceptibility transfer function, are derived using state-space analysis. A design example is provided and the simulations together with experimental results validate the theorical part. To demonstrate the suitability of the proposed structure for *PV* applications a *PV* system incorporating the new converter is presented, focusing on its performance under varying irradiance and temperature conditions. A maximum power point tracking (*MPPT*) algorithm, based on the Perturb and Observe (*P&O*) method, is implemented, and the system is validated through both simulations and experiments. Conclusions and remarks are summarized at the end of the paper, [19].

The proposed converter was developed by modifying the step-up hybrid Boost-*L* converter with switching structure *Up3* from [7]. By coupling the inductors, a simpler topology was achieved. Additionally, diode D_1 was removed since it remains off when the transformer ratio is less than unity, further simplifying the circuit, as shown in Figure 2.123.

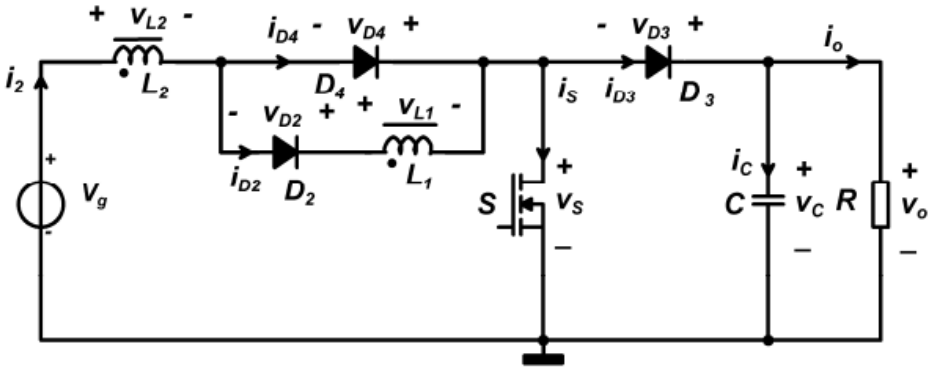

Figure 2.123 The new proposed hybrid inductor-based Boost converter.

This modification reduces the number of components, making the converter more cost-effective and compact compared to those in [7], [52]. The resulting converter consists of one active switch, three passive switches, two coupled inductors, and one output capacitor.

To facilitate the *DC* analysis, a simplified schematic is shown in Figure 2.124, where the perfectly coupled inductors are represented by an ideal transformer (*IT*) with a magnetizing inductor, L_M. The transformer ratio is denoted as n. In this configuration, the magnetizing inductor L_M is connected between the transistor's drain and the cathode of diode D_2, with its value equal to L_1 .

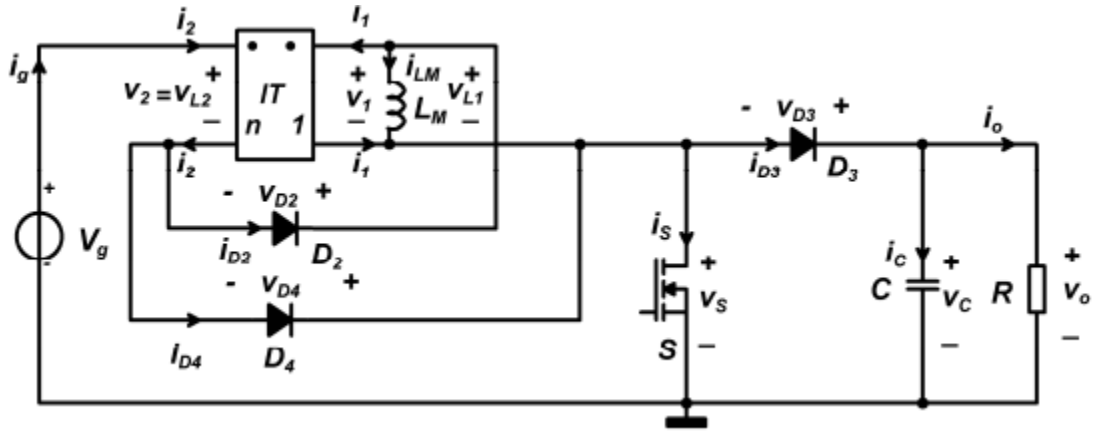

Figure 2.124 Simplified schematic of the proposed hybrid inductor-based Boost converter.

In the first topological state transistor S and diode D_4 are *on*, the other two diodes being *off*, and in the second topological state diodes D_2 and D_3 are *on*, while transistor S and diode D_4 are *off*.

The ideal static conversion ratio M of the new hybrid inductor-based Boost converter is:

$$M = \frac{D+n}{n\cdot(1-D)} \qquad (2.87)$$

The static conversion ratio analysis reveals that the output voltage is higher than the input voltage, confirming the converter step-up functionality. Figure 2.125 illustrates the dependency of the static conversion ratio on the duty cycle, with n as a parameter, where $n<1$. According to Equation (2.87) and Figure 2.125, the proposed hybrid Boost converter with coupled inductors is particularly suitable for applications requiring a significant difference between input and output voltages while maintaining moderate duty cycles. This static conversion ratio exceeds that of the hybrid Boost converter from [7] and the coupled-inductor hybrid Boost converter from [11] at the same duty cycle, provided if the transformer ratio n is less than unity. For $n=1$, the static conversion ratio simplifies to $(1+D)/(1-D)$, identical to the converters in [7] and [11].

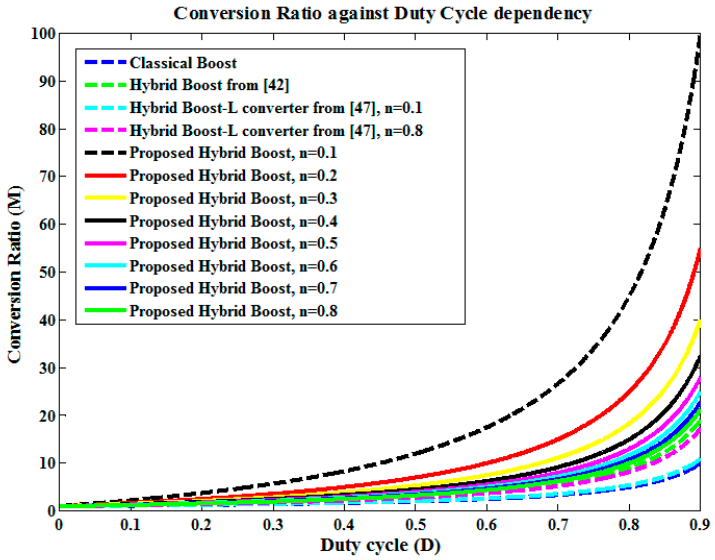

Figure 2.125 Static conversion ratio against duty cycle for the proposed converter (where n = 0.1–0.8), classical Boost converter, Hybrid Boost converter from [7] and Hybrid Boost-*L* converter from [11].

After analysing the converter and writing the main equations, the state space analysis and model with lossy elements is developed.

State space analysis

The dynamics of the proposed ideal inductor-based Boost converter are analysed using the state-space approach. Defining the state vector $x = \begin{bmatrix} i_{LM} \\ v_C \end{bmatrix}$, the input vector $u = [v_g]$, and output vector $y = [v_o]$, the state matrices for the first topological state are:

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{R \cdot C} \end{bmatrix}; \quad \mathbf{B}_1 = \begin{bmatrix} \dfrac{1}{n \cdot L_M} \\ 0 \end{bmatrix}; \quad \mathbf{E}_1 = [0 \quad 1]; \quad F_1 = [0]; \tag{2.88}$$

In the second topological state, the state matrices for the converter are as follows:

$$\mathbf{A}_2 = \begin{bmatrix} 0 & -\dfrac{1}{(n+1) \cdot L_M} \\ \dfrac{1}{(n+1) \cdot C} & -\dfrac{1}{R \cdot C} \end{bmatrix}; \quad \mathbf{B}_2 = \begin{bmatrix} \dfrac{1}{(n+1) \cdot L_M} \\ 0 \end{bmatrix}; \quad \mathbf{E}_2 = [0 \quad 1]; \quad \mathbf{F}_2 = [0]; \tag{2.89}$$

The static conversion ratio was symbolically calculated in MATLAB™ [54] to verify the accuracy of the previous analytical derivations. The formula employed for determining the static conversion ratio is provided in [73]:

$$\mathbf{M} = F_D - E_D \cdot A_D^{-1} \cdot B_D \tag{2.90}$$

$$\begin{cases} \mathbf{A}_D = D \cdot A_1 + (1-D) \cdot A_2 \\ \mathbf{B}_D = D \cdot B_1 + (1-D) \cdot B_2 \\ \mathbf{E}_D = D \cdot E_1 + (1-D) \cdot E_2 \\ \mathbf{F}_D = D \cdot F_1 + (1-D) \cdot F_2 \end{cases} \quad (2.91)$$

After performing the calculations in MATLAB, the resulting static conversion ratio is the same as that in Equation (2.87).

$$M = \frac{D+n}{n \cdot (1-D)} \quad (2.92)$$

The small-signal transfer functions are derived by averaging and linearizing the switched equations [73]. The control-to-output transfer function is:

$$G_c(s) = \frac{\hat{V}_o(s)}{\hat{d}(s)} \quad (2.93)$$

$$G_c(s) = V_g \cdot \frac{n+1}{n} \cdot \frac{1}{(1-D)^2} \cdot \frac{1 - \frac{L_M}{R} \cdot \frac{(D+n)\cdot(n+1)}{(1-D)^2} \cdot s}{1 + \frac{L_M}{R} \cdot \frac{(n+1)^2}{(1-D)^2} \cdot s + L_M \cdot C \cdot \frac{(n+1)^2}{(1-D)^2} \cdot s^2} \quad (2.94)$$

and the audiosusceptibility,

$$G_g(s) = \frac{\hat{V}_o(s)}{\hat{V}_g(s)} \quad (2.95)$$

$$G_g(s) = \frac{\frac{D+n}{n \cdot (1-D)}}{1 + \frac{L_M}{R} \cdot \frac{(n+1)^2}{(1-D)^2} \cdot s + L_M \cdot C \cdot \frac{(n+1)^2}{(1-D)^2} \cdot s^2} \quad (2.96)$$

This dynamic model serves as the basis for feedback loop design. Both transfer functions are of second order, and the control-to-output transfer function features a zero in the right half-plane. Consequently, the behaviour resembles that of a classical Boost converter. Therefore, the controller can be designed using the same approach, using for example a third order error amplifier [74]

Model with Lossy Elements

This model incorporates a more accurate representation of the converter components by considering the effect of conduction losses. The equivalent circuit, shown in Figure 2.126, includes lossy elements such as the transistor on-resistance R_{ON} and the forward voltage drops of the diodes, V_{D2}, V_{D3} and V_{D4}.

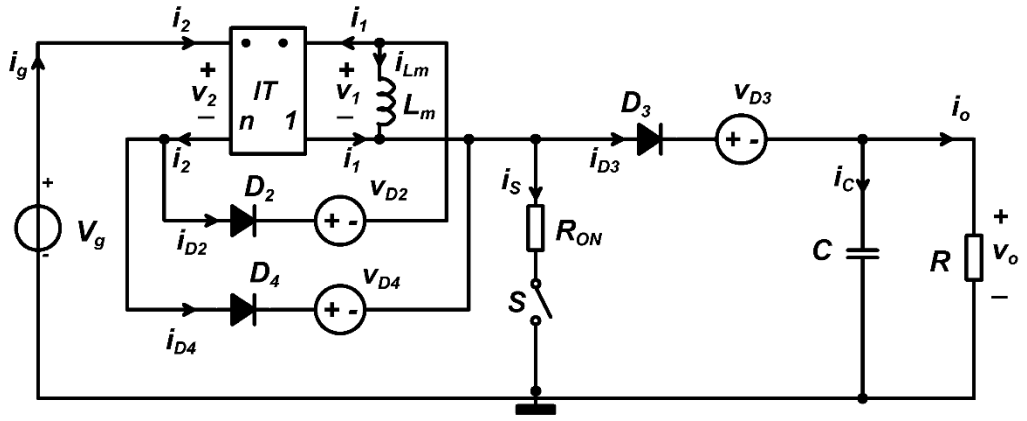

Figure 2.126 Simplified schematic of the proposed hybrid inductor-based Boost converter with lossy elements.

Based on the converter's operating principle, the voltages across the magnetizing inductor during the *ON* and *OFF* states are:

$$v_{LM\_ON} = \frac{n \cdot V_g - R_{ON} \cdot I_{LM} - n \cdot V_{D4}}{n^2} \quad (2.97)$$

$$v_{LM\_OFF} = \frac{-V_{D2} - V_{D3} + V_g - V_C}{n+1} \quad (2.98)$$

and applying volt-second balance principle it results that:

$$D \cdot \frac{n \cdot V_g - R_{ON} \cdot I_{LM} - n \cdot V_{D4}}{n^2} + (1-D) \cdot \left(\frac{-V_{D2} - V_{D3} + V_g - V_C}{n+1} \right) = 0 \quad (2.99)$$

Using symbolic calculations in MATLAB, the output voltage of the converter, taking into account the conduction losses, is obtained as:

$$V_C = \frac{\frac{n+D}{n \cdot (1-D)} \cdot V_g - V_{D2} - V_{D3} - \frac{(n+1) \cdot D}{n \cdot (1-D)} \cdot V_{D4}}{1 + \left(\frac{n+1}{n} \right)^2 \cdot \frac{D}{(1-D)^2} \cdot \frac{R_{ON}}{R}} \quad (2.100)$$

Design example of the proposed converter

The proposed converter is utilized in a PV panel system to implement *MPPT*. Consequently, the design specifications of the converter are determined based on the characteristics and requirements of the *PV* module.

For the experiments, two *PV* modules were connected in series to increase the input voltage. The *PV* module used was the MWG-20 model from MW GREEN POWER, with the following specifications for each module:

- Peak power: $P_{max} = 20$ W
- Maximum power point current: $I_{mp} = 1.14$ A
- Maximum power point voltage: $V_{mp} = 17.49$ V
- Short circuit current: $I_{sc} = 1.22$ A
- Open circuit voltage: $V_{oc} = 21.67$ V

These values are obtained in standard test conditions of solar irradiance and temperature: $G = 1000$ W/m^2 and $T = 25$ °C.

- The input voltage range was between: $V_g = 30 \div 35$ V
- Maximum output power: $P_o = 40$ W
- Switching frequency: $f_s = 100$ kHz
- Output voltage: $V_o = 120$ V

From the calculations presented in detail in the paper, the obtained values are: the transformer turn ratio resulted to be 0.567 and the calculated duty cycle range resulted between 0.46 and 0.52. For the practical prototype a resistive load of 432 Ω was used. The calculated inductor value was $L_M = 2$ mH. The value of L_M will be equal to the value of L_1, so $L_M = L_1 = 2$ mH, and $L_2 = n^2 L_M = 644$ µH. The capacitor value is $C = 10$ µF. The transistor voltage stress is $V_s = 120$ V and its dc current is $I_S \sim 1$ A. The highest stresses for diodes are a reverse voltage of $V_D = 120$ V, and the dc current $I_D \sim 1$ A. The semiconductors used were: transistor S = Infineon Mosfet IPB073N15N5 and diodes $D_{2,3,4}$ =ROHM super-fast recovery diode RFN10NS6SFH. The MOSFET driver was 1EDN7512BXTSA1 from Infineon.

The simulations and experimental results Figure 2.127 and Figure 2.128, were conducted using a DC source in place of a PV panel, to verify the converter functionality.

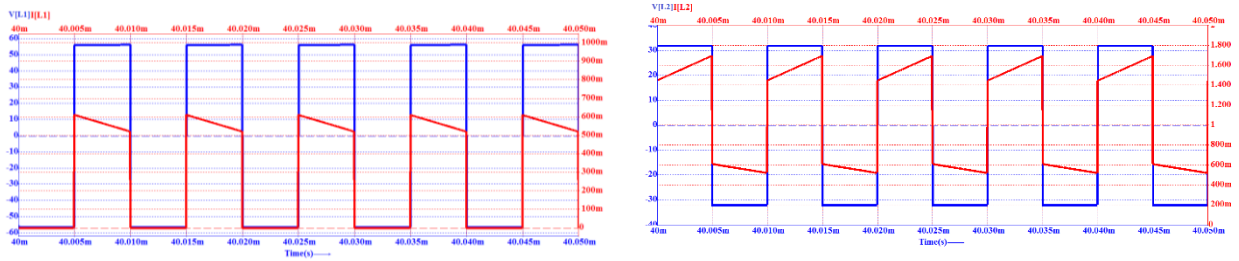

Figure 2.127 Voltage and current corresponding to the primary and secondary of the transformer.

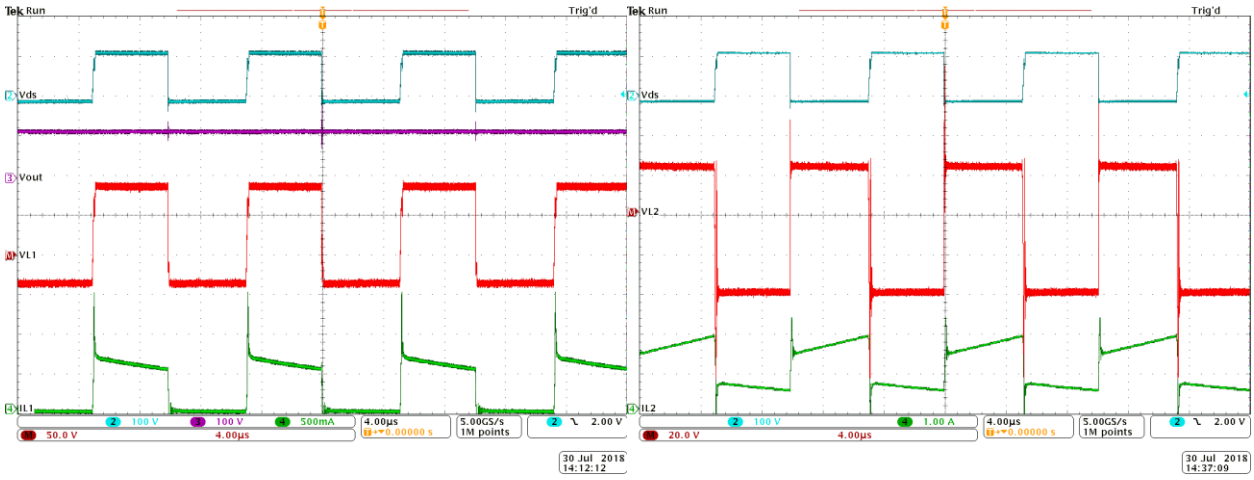

Figure 2.128 Oscilloscope waveforms: in the left - transistor drain to source voltage (cyan - V_{ds}); output voltage (magenta - V_{out}); voltage across the primary winding (red - v_{L1}); current in the primary winding (green - i_{L1}); in the right transistor drain to source voltage (cyan - V_{ds}); voltage across the secondary winding (red - v_{L2}) and current in the secondary (green - i_{L2}).

The waveforms closely match the theoretical predictions and simulation results, both qualitatively and quantitatively.

The dc input and output currents, along with the dc output voltage, were measured using a digital multimeter (*DMM*). Figure 2.129, in the left, shows the comparison of the *DC* conversion ratio between the experimental curve and the theoretical ideal curve, while in the right the computed efficiency results are presented.

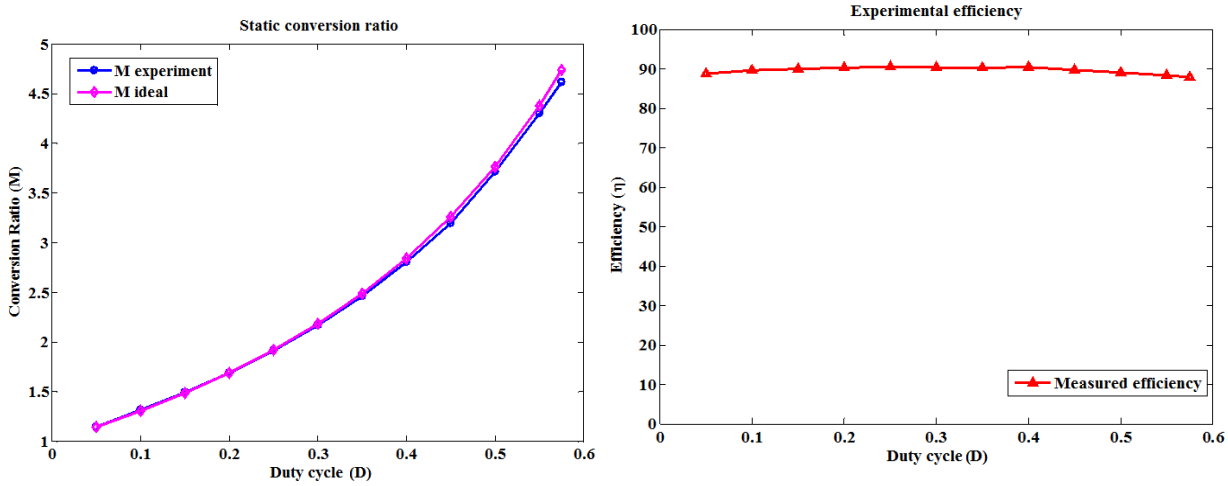

Figure 2.129 The experimental conversion ratio against duty cycle in comparison to the ideal one in the left and in the right side the experimental efficiency against the duty cycle.

The measured conversion ratio closely matches with the ideal characteristic, and a high efficiency of approximately 90% is achieved.

Application of the proposed converter in a PV system for performing the MPPT

The block diagram of the PV system is illustrated in Figure 2.130.

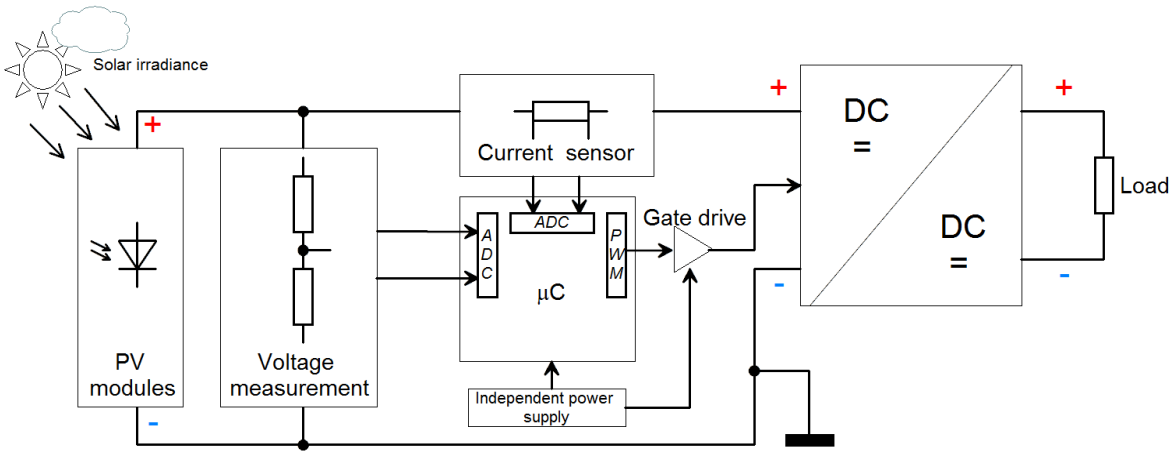

Figure 2.130 Block diagram of the PV energy system.

For practical implementation of the maximum power point (*MPP*) algorithm, an ADuCino development board equipped with the ARM microcontroller ADuCM360 was selected, [75]. This

microcontroller was chosen for its ability to simultaneously sample the current and voltage from the *PV* modules. The current was measured using a *LEM HO-8-NSM/SP33* transducer with three turns, providing a nominal measurement current of 8/3A. The voltage across the *PV* modules is measured using a resistive divider, which is differentially connected to the ADC. Precision resistors with a tolerance of 0.1% were employed for accurate measurements. The Cortex-M3 core supports 32-bit calculations, ensuring efficient processing. Additionally, the sensors and gate driver are compatible with the microcontroller 3.3V supply voltage, eliminating the need for level shifters.

The software flow chart, Figure 2.131, begins with the initialization of the clock system, along with the required modules: ADC, PWM, Universal Asynchronous Receiver Transmitter (UART), TIMER, and the MPPT algorithm.

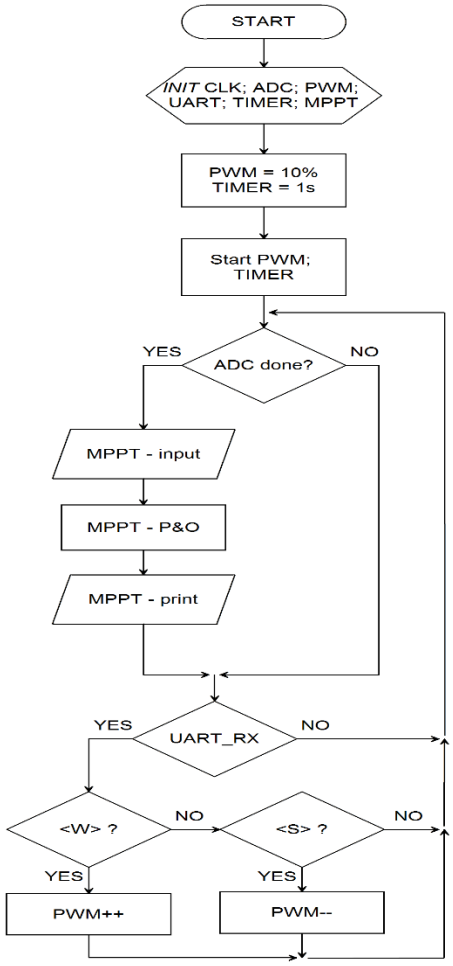

Figure 2.131 Main flowchart.

The PWM starts with an initial duty cycle of 10%, and the TIMER is configured to generate interruptions at a 1-second interval, waiting for the ADC conversion results. The MPPT algorithm employs the Perturb and Observe (P&O) strategy [76], [77], [78], [79], [80], [81], [82], [83], [84], as detailed in the subroutine flowchart shown in Figure 2.132.

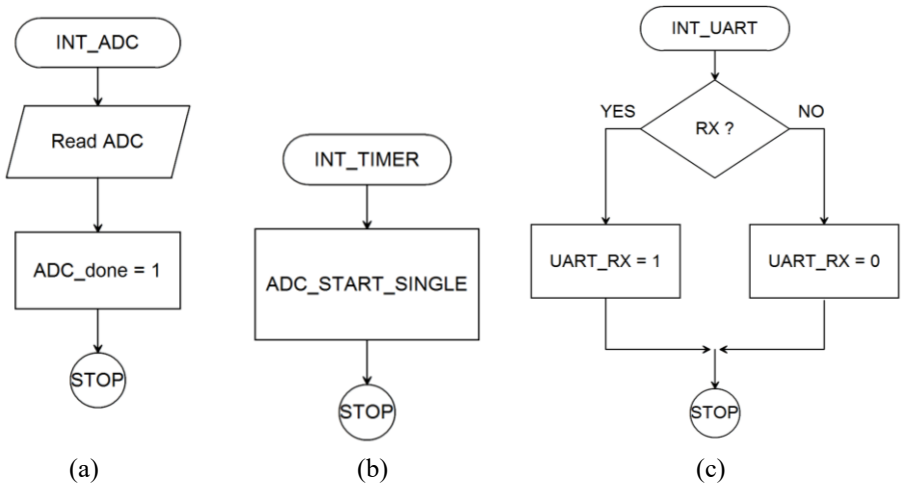

Figure 2.132 Subroutine flowchart: (a) ADC reading subroutine; (b) TIMER subroutine; (c) UART message receiving subroutine.

The flowchart of the MPPT algorithm with P&O is detailed in Figure 2.133.

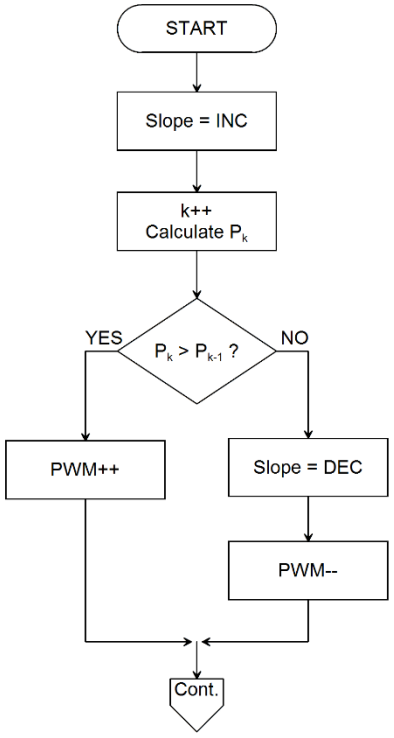

Figure 2.133 MPPT algorithm implementation flowchart.

The minimum and maximum duty cycle limits, that cannot be exceeded, are defined as constants during the software initialization.

Simulation of the MPPT algorithm using the proposed hybrid inductor-based Boost converter in a PV system

Simulations using CASPOC were conducted to trace the characteristic curves of PV modules under varying irradiance levels of 600, 800, and 1000 W/m², marked with (0), (1) and (2), respectively in Figure 2.134, at a temperature of T_a = 60 °C. At 1000 W/m², the maximum power was 36.16 W, with V = 30.73 V, I = 1.17 A, I_{sc} = 1.292 A and V_{oc} = 38.02 V. For 800 W/m², the maximum power was 28.25 W, with V=29.60 V, I=0.95 A, I_{sc} = 1.048 A, and V_{oc} = 36.62 V. At 600 W/m², the maximum power was 20.61 W, with V = 28.15 V, I = 0.73 A, I_{sc} = 0.804 A and V_{oc} = 34.82 V. The results demonstrate how power, voltage, and current vary with irradiance.

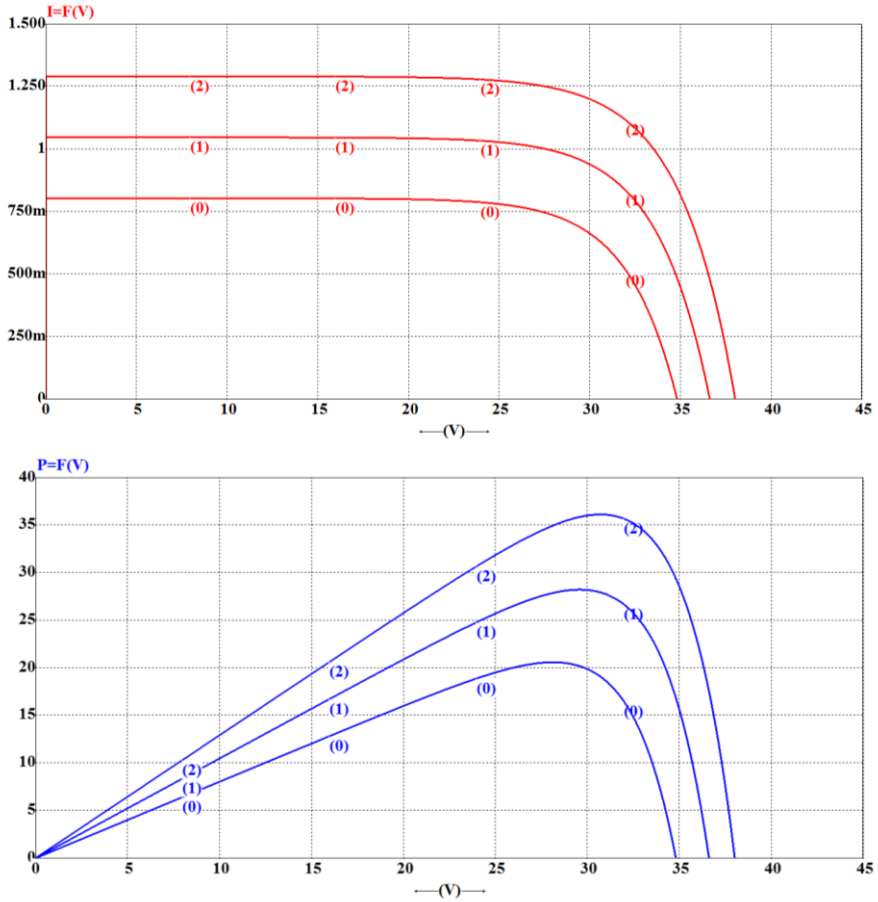

Figure 2.134 Current-voltage characteristics and power characteristics of the PV module.

A simulation of the proposed hybrid step-up converter was conducted using the same component values and *PV* panel characteristics as in the practical circuit. Figure 2.135 shows the input-output power characteristic, where a transient start-up mode occurs till approximately 100 ms. At T_1 = 233 ms, a step change in irradiance from G_1 = 1000 W/m^2 to G_2 = 800 W/m^2 is applied, followed by a return to G_3 = 1000 W/m^2 at T_2 = 385 ms. The MPPT control loop adjusts the power absorbed from the panel to approximately 34.5 W under an irradiance equals to 1000 W/m^2. This demonstrates the converter capability to adapt to changing irradiance levels.

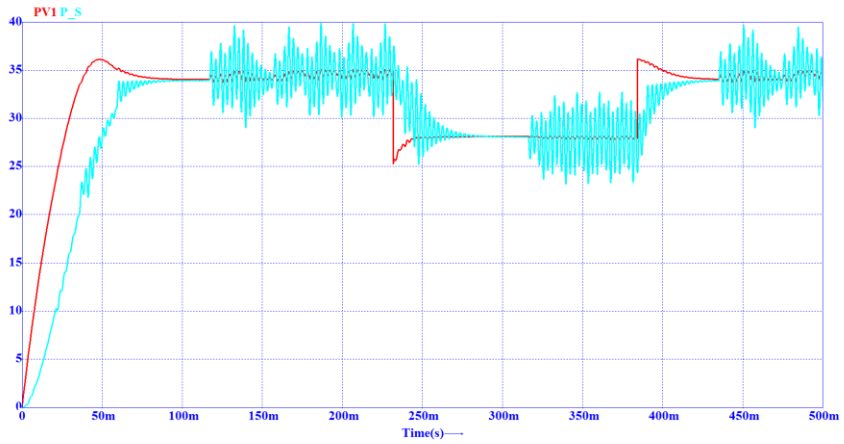

Figure 2.135 Simulation of input and output power evolution in time.

In, the arrow extends beyond the maximum power point at the end of the simulation due to the P&O control strategy. The green arrow indicates the operating point position on the current-voltage characteristic, tracking the transition before and after the maximum point.

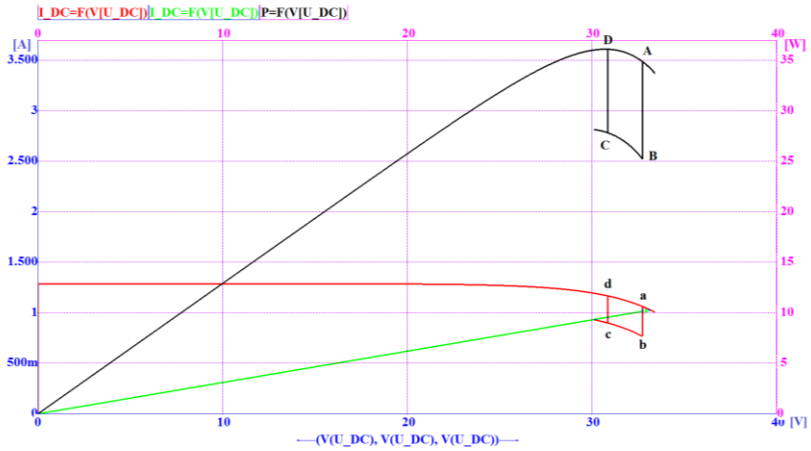

Figure 2.136 Simulation of current-voltage and output power characteristics with MPPT and P&O.

Figure 2.137 shows the duty cycle generated by the *P&O* algorithm, settling around 0.49 after the 100 ms transient period. Figure 2.138 confirms that the desired average voltage of 120 V is achieved. The simulation ran for 500 ms, with a 100 ns step size, and the results were displayed every five samples.

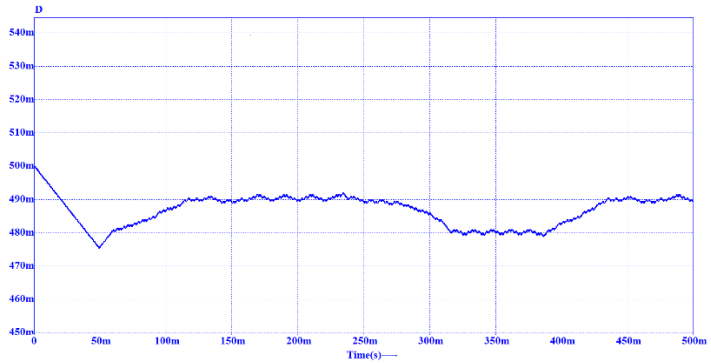

Figure 2.137 Duty cycle evolution.

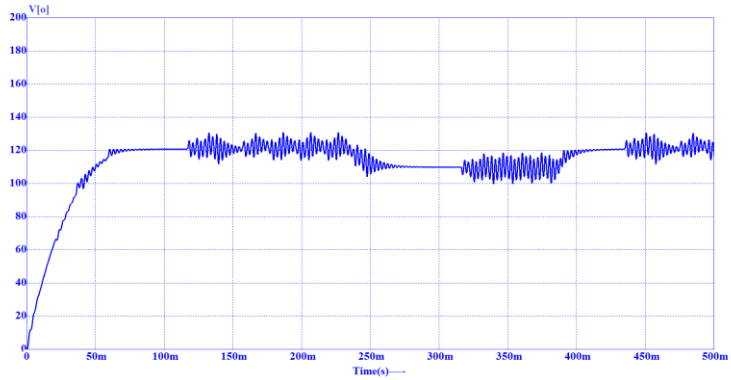

Figure 2.138 Output voltage.

These figures illustrate the correlation between the power characteristic, voltage characteristic, and duty cycle.

Practical results of the MPPT algorithm using the proposed hybrid inductor-based Boost converter

Functional tests of the proposed converter, integrated with a *PV* system and *MPPT* controller algorithm were conducted under constant and variable solar irradiance conditions. In Figure 2.139, under 720 W/m², the system enters steady state after 4 seconds from startup, with the *P&O* algorithm maintaining the operating point close to the *MPP*. The output voltage settles at 120 V, while input power and current reach steady-state values of 34 W and 1.1 A, respectively. Figure 2.139 right highlights the *MPPT* steps during startup under 852 W/m², showing smooth operation without overshoot as the converter adjusts the duty cycle to maximize power.
Figure 2.140 left explores the effects of a passing cloud, causing irradiance and corresponding power drops. Despite these changes, the controller successfully tracks the *MPP*, as evident from the input characteristic Figure 2.140 right, which shows the transitions between curves for different irradiance levels. Figure 2.141 left illustrates performance under a dense cloud, with the irradiance dropping to 100 W/m². The efficiency remains high, even with reduced sunlight, demonstrating the system robustness. The XoY chart in Figure 2.141 right confirms the controller maintains the operating point along the MPP line, proving the digital controller design and implementation are effective. Overall, the proposed system is a reliable solution for solar energy harvesting.

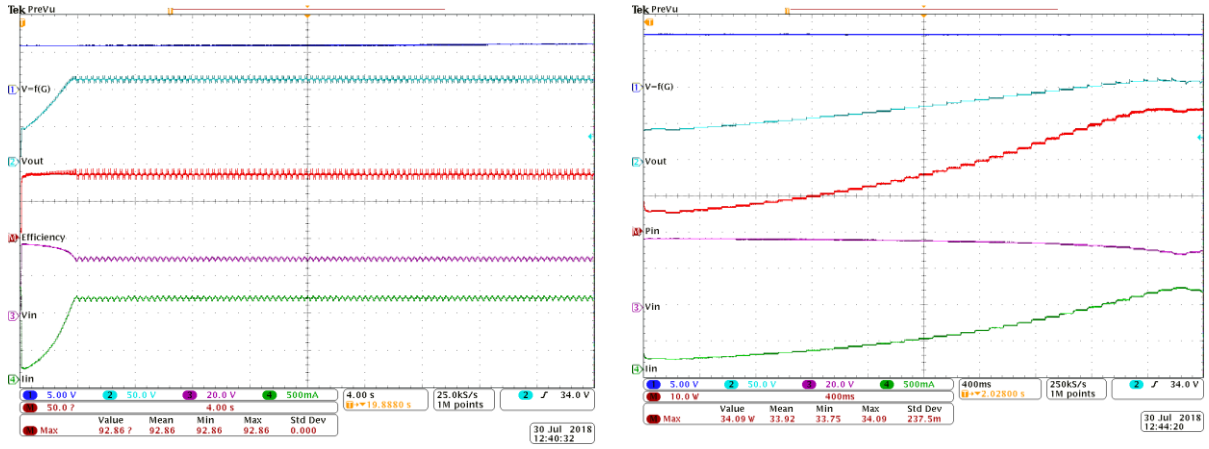

Figure 2.139 Main converter waveforms and efficiency from start-up to steady state in sunny conditions: irradiance, output voltage, efficiency, input voltage and input current, this up to down order.

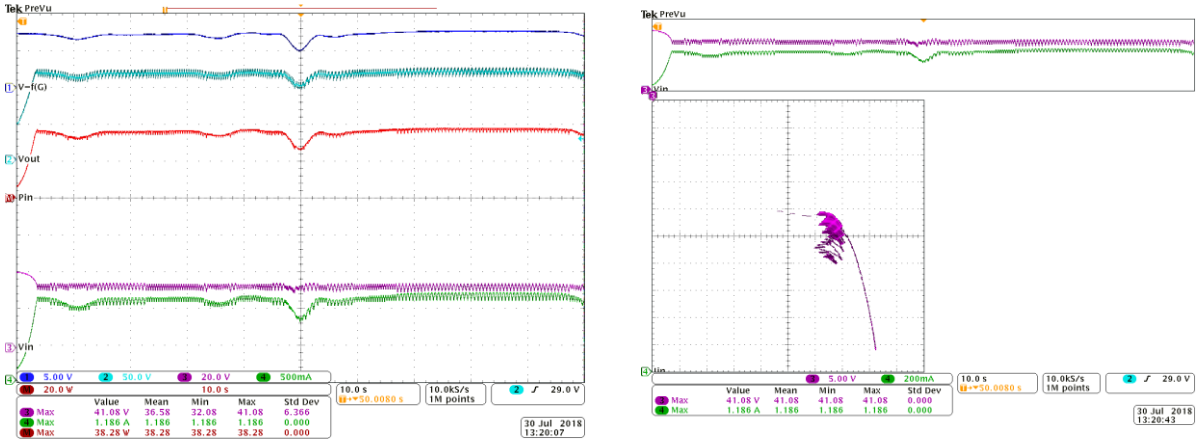

Figure 2.140 Main converter waveforms during a small and transparent cloud occurrence: irradiance, output voltage, input power, input voltage and input current, this up to down order, left. Input characteristic corresponding to: Input current is in *oX* axis and input voltage on the *oY* axis, right.

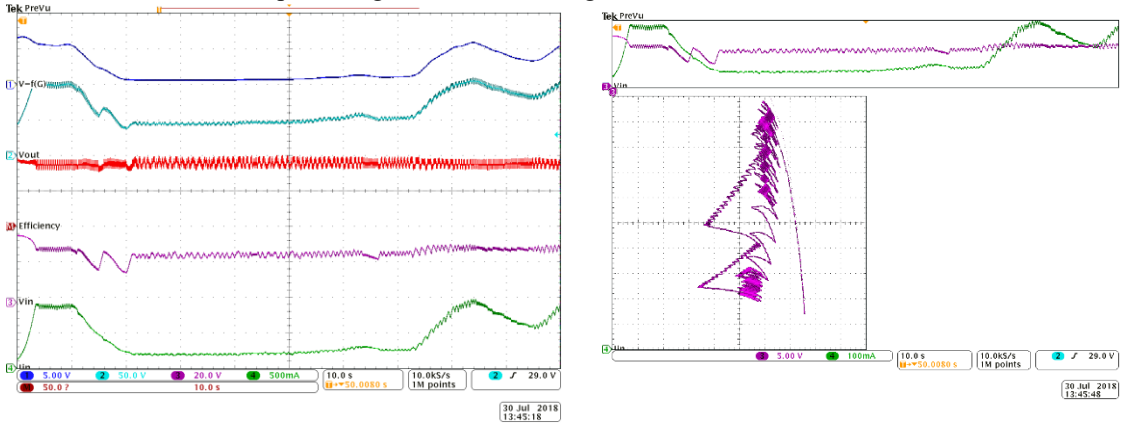

Figure 2.141 Main converter waveforms during a small but dense cloud occurrence: irradiance, output voltage, input power, input voltage and input current, this up to down order-left; Input current is on *oX* axis and input voltage on the *oY* axis - right.

Conclusions

The proposed hybrid inductor-based boost converter offers a high step-up conversion ratio, reduced component count compared to other hybrid structures, and excellent performance under varying environmental conditions. Its integration with *PV* systems, supported by a robust *MPPT* algorithm, demonstrates its viability as an efficient and cost-effective solution for solar energy harvesting. The study successfully bridges theoretical modelling, simulation, and practical experimentation, proving the converter potential for renewable energy applications.

2.1.3.2 SEPIC-based DC-DC converter with coupled inductors suitable for high step-up applications

The paper entitled "A New SEPIC-Based DC-DC Converter with Coupled Inductors Suitable for High Step-Up Applications", [30], presents a novel hybrid SEPIC-based DC-DC converter with coupled inductors, specifically designed for photovoltaic applications. The converter achieves higher step-up ratios and reduced component stresses compared to classical, [55], and hybrid SEPIC topologies, [7]. Steady-state equations, static conversion ratio, and *CCM* operation conditions were derived for performance analysis. Theoretical validation was conducted using Caspoc simulations, and a prototype confirmed feasibility and practical efficiency, achieving over 90% efficiency. A comparative study demonstrated the converter's advantages, such as simplified design and better performance at moderate duty cycles. Integrated into a solar energy system, it successfully implemented a MPPT algorithm, optimizing energy conversion. The results highlighted the converter potential for high step-up photovoltaic applications, improved efficiency and reduced complexity. The paper is presented in detail in [30]. The design of this topology started from the hybrid SEPIC converter featuring the Switching Up 3 structure from [7], that was analysed in detail in [7], [85] and presented in Figure 2.142.

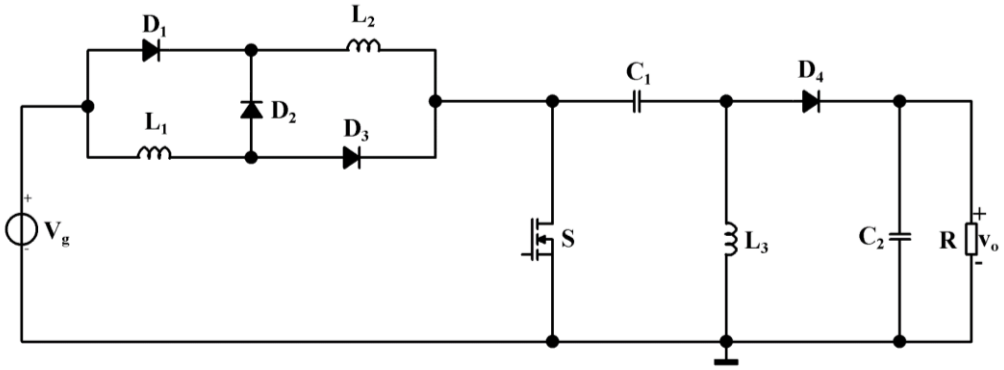

Figure 2.142 SEPIC hybrid converter with a switching Up 3 structure presented in [7].

The proposed converter was developed by coupling inductors L_1 and L_2, a technique previously employed by the authors in other research [22], [19], [9] and [23]. Assuming ideal coupling, the transformer ratio n the operation is analysed for cases with $n<1$. In this configuration, diode D_3 is always *off* and can be removed, simplifying the topology. The resulting design, shown in Figure 2.143, is more cost-effective, requiring one active switch, three passive switches, an individual inductor, and a pair of coupled inductors with one internal and one output capacitor. The converter analysis assumes ideal components, modelling the coupled inductors as an ideal transformer with a magnetizing inductor L_M, equal to L_1, as shown in Figure 2.144, with all

evaluations based on *CCM* operation. In the first topological state transistor *S* and diode D_1 are on, while in the second topological state only diodes D_2 and D_4 are on.

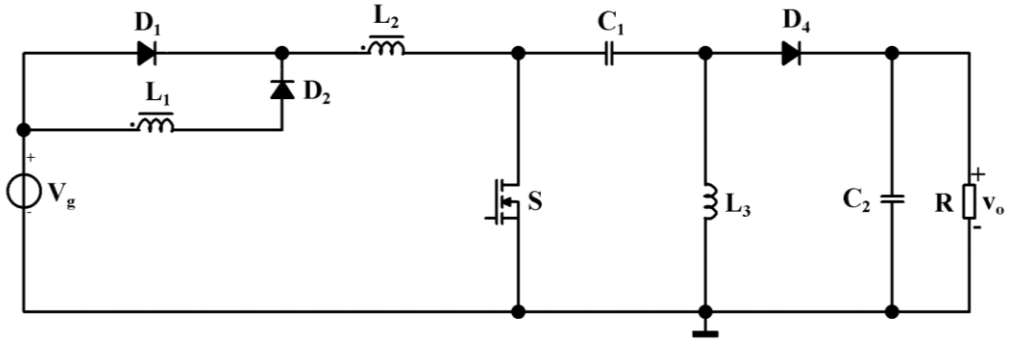

Figure 2.143 The proposed hybrid SEPIC-based converter with coupled inductors.

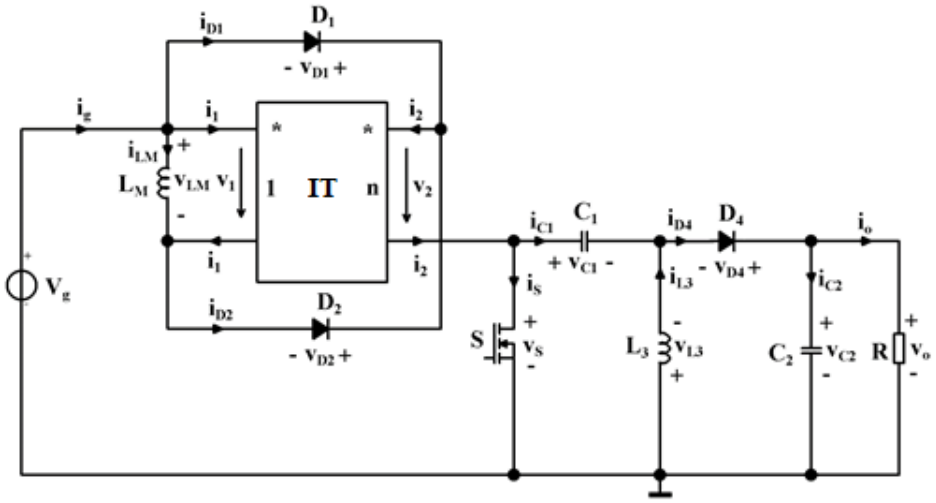

Figure 2.144 Equivalent schematic of the proposed hybrid SEPIC-based dc-dc converter with coupled inductors.

The ideal static conversion ratio is:

$$M = \frac{D}{1-D} \cdot \frac{n+D}{n} \qquad (2.101)$$

From Equation (2.101), the duty cycle can be derived as a function of the static conversion ratio and the transformer ratio *n*, resulting in a second-degree equation.

$$D = \frac{-n\cdot(1+M)\cdot\left(\sqrt{n^2\cdot(1+M)^2+4\cdot n\cdot M}\right)}{2} \qquad (2.102)$$

For *CCM* operation, all diodes must remain on during their designated conduction states, requiring positive minimum diode currents. For diodes D_1 and D_2, the *CCM* condition is $I_{LMmin} \geq 0$, where $I_{LMmin} = I_{LM} - \frac{1}{2}\Delta I_{LM} \geq 0$. For diode D_4, the condition is $\frac{I_{LMmin}}{1+n} + I_{L3min} > 0$, with $I_{LMmin} = I_{LM} - \frac{1}{2}\Delta I_{LM}$ and $I_{L3min} = I_{L3} - \frac{1}{2}\Delta I_{L3}$. Finally, the *CCM* conditions are:

$$\frac{2\cdot L_M\cdot f_S}{R} \geq \frac{(1-D)^2}{D\cdot(n+D)\cdot(1+n)} \qquad (2.103)$$

$$\frac{2 \cdot L_e \cdot f_S}{R} \geq \frac{(1-D)^2}{n+D} \quad (2.104)$$

where the equivalent inductor L_e is $L_e = \left(L_M \cdot (n+D)\right) || \frac{L_3}{1+n}$.

Figure 2.145 illustrates the relationship between the static conversion ratio and the duty cycle for the classical isolated SEPIC [86], the hybrid SEPIC [7], and the proposed hybrid SEPIC-based converter, with a detailed view for duty cycles in the range [0–0.5] for clearer comparison.

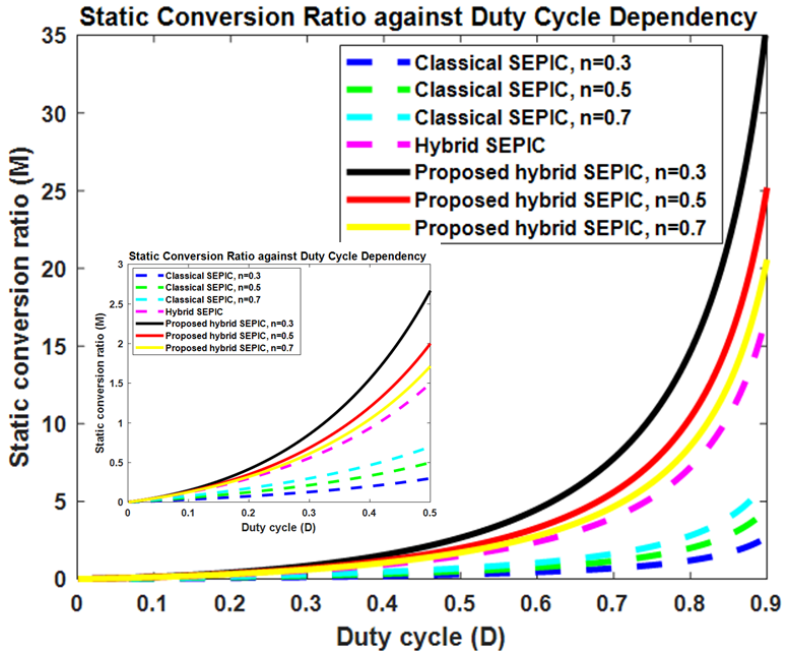

Figure 2.145 Static conversion ratio against the duty cycle for the classical isolated SEPIC, hybrid SEPIC and proposed converter with the turns ratio as a parameter.

The proposed SEPIC converter exhibits both step-down and step-up capabilities, achieving a higher static conversion ratio at lower duty cycles compared to the isolated and hybrid SEPIC converters. Figure 2.145 also shows that a lower transformer ratio n enhances the step-up capability, making the converter ideal for applications requiring a significant input-to-output voltage difference.

The theoretical waveforms associated to the converter are presented in Figure 2.146.

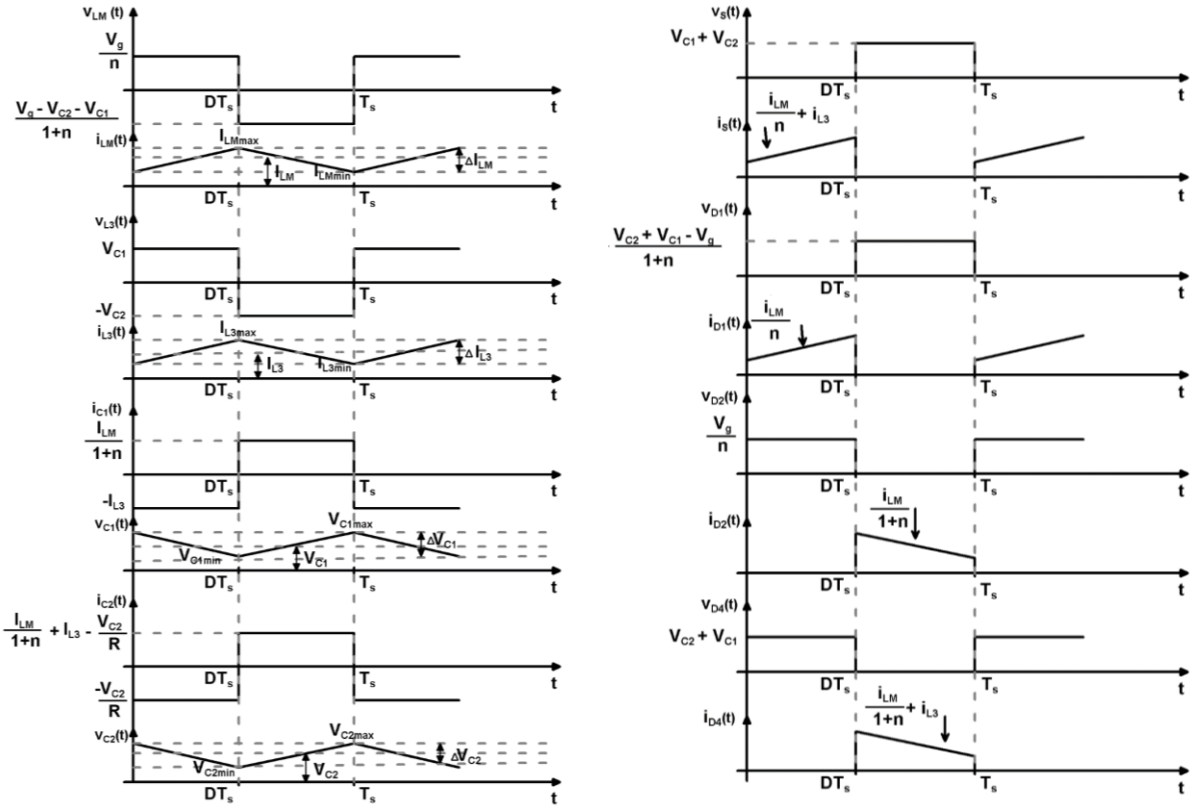

Figure 2.146 Main waveforms associated to the proposed converter: the passive components – left, and the semiconductor devices – right.

Design example for the proposed converter

The converter being used in a PV system, the requirements for the proposed SEPIC converter depend on the PV panel characteristics. Two PV modules MWG-20 connected in series were used for experiments, with the characteristics described also in the previous paragraph, paper [19].
The converter was designed according to the following parameters:

- The input voltage range $V_g = 30 \div 35$ V correlated to V_{mp}
- Maximum output power: $P_o = 40$ W
- Switching frequency: $f_s = 100$ kHz
- Output voltage: $V_o = 120$ V
- Output voltage peak-to-peak ripple: $\Delta V_{C2} = 300$ mV
- Transformer ratio: $n = 0.5$.

After some calculations, the minimum and maximum static conversion ratios are 3.42 and 4, respectively. The necessary duty cycle range will result in $D \in [0.6070, 0.6375]$. The load resistor is 360Ω.

The calculated minimum values for the converter components are $L_M = L_1 = 1.7$ mH, $L_2 = 425$ µH, $L_{3min} = 5200$ µH, $C_{1min} = 0.26$ µF and $C_{2min} = 6.72$ µF. Laboratory-manufactured components yielded practical values of $L_1 = 2$ mH, $L_2 = 503$ µH and $L_3 = 5900$ µH, with a transformer ratio $n = 0.5014$, and standard capacitor values $C_1 = 0.33$ µF and $C_2 = 10$ µF. Key stress values include transistor voltage $V_S = 197$ V and current $I_S = 1.33$ A, diode D_1 stress $V_{D1} = 108$ V, $I_{D1} = 1.12$ A, diode D_2 stress $V_{D2} = 70$ V and $I_{D2} = 0.21$ A, and diode D_4 stress $V_{D4} = 197$ V and $I_{D4} = 0.33$ A.

Simulations and experimental results

A simulation of the ideal SEPIC-based DC-DC converter with coupled inductors was conducted using Caspoc software to validate the theoretical design. Using component values from the design example, with $V_g = 30$ V, a static conversion ratio $M = 4$, and a duty cycle $D = 0.6375$, the simulation predicted an output voltage V_o=120 V, Figure 2.147 left, validates the theoretical calculations. The triangular magnetizing current shape was confirmed in Figure 2.147 right, while voltages and currents for L_3, Figure 2.149 validated correct *CCM* operation. Voltage and current waveforms for the coupled inductors L_1 and L_2 are also presented in Figure 2.148.

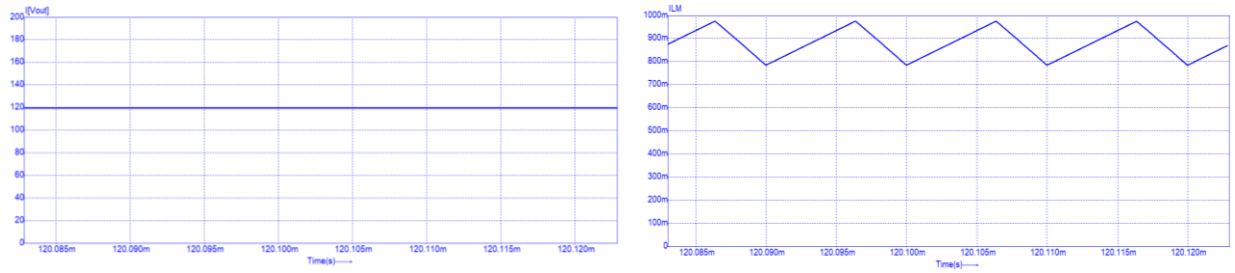

Figure 2.147 Output dc voltage – left, and magnetizing inductor current i_{LM} -right.

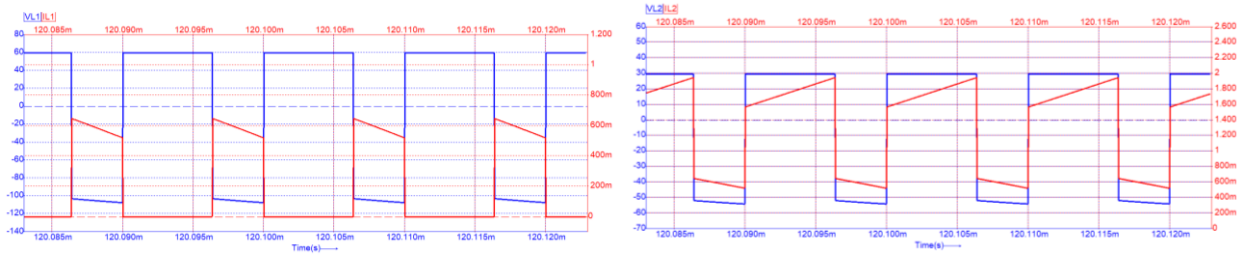

Figure 2.148 Voltage (blue) and current (red) of the primary winding L_1 – left, and of the secondary winding L_2 - right

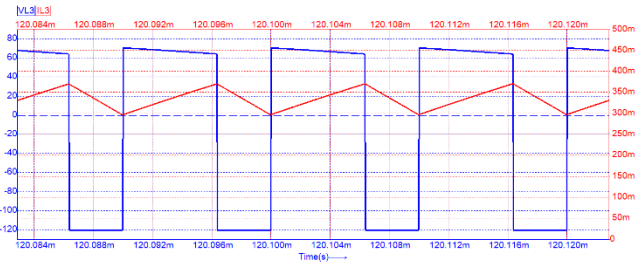

Figure 2.149 Voltage (blue) and current (red) for the inductor L_3.

A prototype of the proposed SEPIC converter was built to validate its functionality, using the same design parameters as in the simulation. The semiconductors included an STW70N60M2 transistor and STPSC4H065 silicon carbide diodes. Coupled inductors L_1 and L_2 were constructed on an E71/33/32-3C94 FERROXCUBE core, while L_3 used a separate core. Experimental tests, Figure 2.150, with V_g = 30 V, f_s = 100 kHz, and R = 360 Ω showed waveforms consistent with simulations. Figure 2.151-Figure 2.152 illustrate the voltage and current waveforms across L_1, L_2, and L_3, as well as the output voltage, confirming the prototype accurate performance.

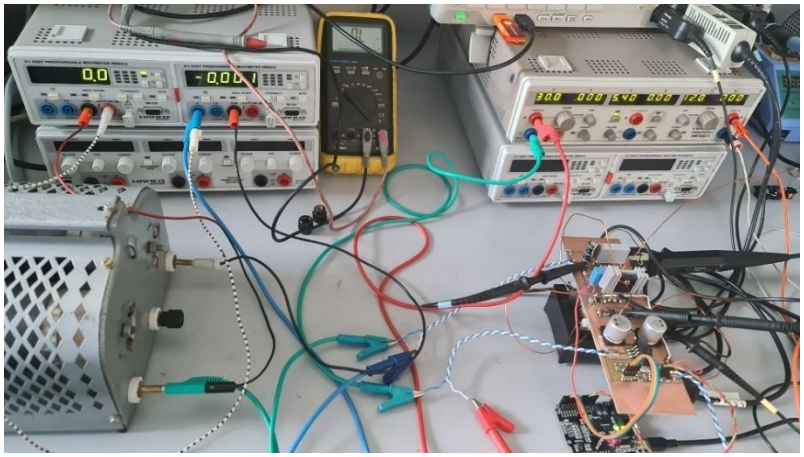

Figure 2.150 View of the experimental setup.

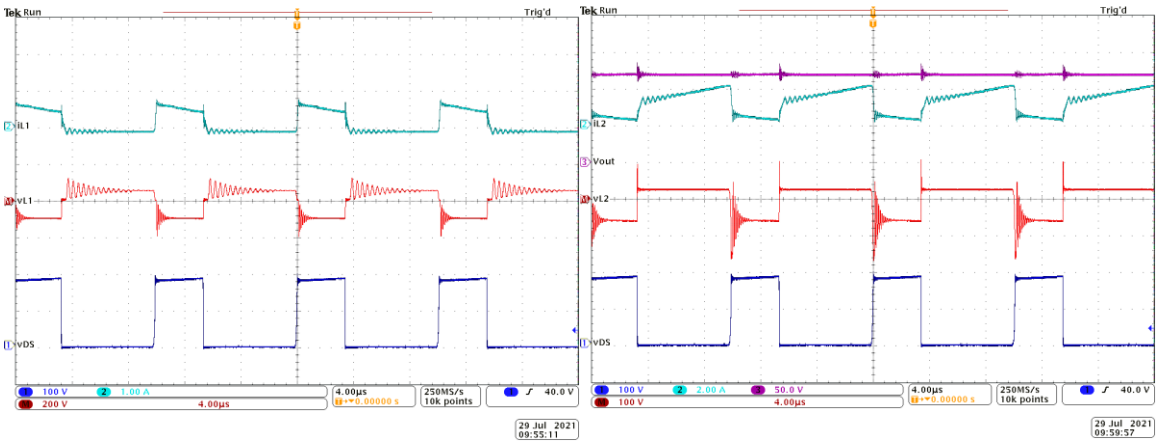

Figure 2.151 Oscilloscope waveforms: drain to source voltage (dark blue—v_{DS}); voltage across L_1 (red -v_{L1}); current through L_1 (cyan—i_{L1}) – left, and drain-to-source voltage (dark blue—v_{DS}); voltage across L_2 (red—v_{L2}); current through L_2 (cyan—i_{L2}) and output voltage (purple—V_{out}) – right.

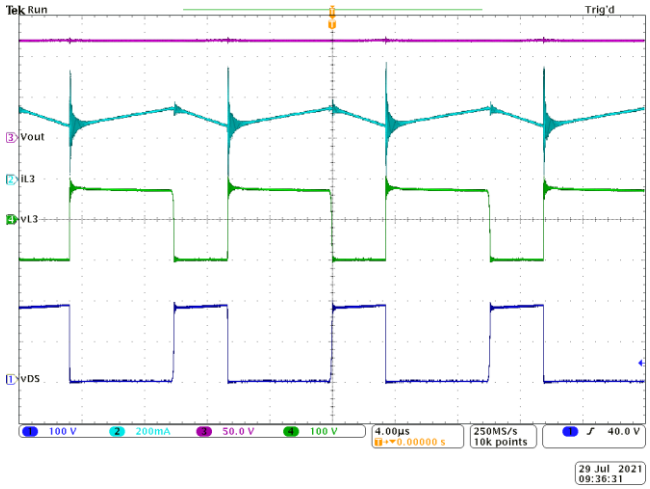

Figure 2.152 Oscilloscope waveforms: drain-to source-voltage (dark blue—v_{DS}); voltage across L_3 (green—v_{L3}); current through L_3 (cyan—i_{L2}) and output voltage (purple-V_{out}).

Applicability of the proposed SEPIC converter in a PV system

To demonstrate the applicability of the proposed SEPIC converter in *PV* applications, a *PV* system was built using a structure similar to that in [19]. The *P&O* algorithm was implemented for MPPT on an ADuCino development board with an ADuCM360 ARM microcontroller. A LEM HO-8-NSM/SP33 current transducer and a resistive divider were used to measure current and voltage across the *PV* modules. The *MPPT* algorithm, detailed in [19], enabled efficient energy harvesting from the *PV* system.

A simulation was conducted to evaluate the proposed SEPIC converter in a PV system under various step changes in irradiance and load resistance over 250 ms. Key events included changes in irradiance (G = 1000 W/m^2 to G = 800 W/m^2 and back) and load resistance (R varying from 450 Ω to 360Ω). The MPPT algorithm effectively regulated the absorbed power, maintaining approximately 40 W at G = 1000 W/m^2, 30 W at 800 W/m^2, and 35 W at 900 W/m^2.
Figure 2.153 illustrates the input and output power evolution, confirming the system ability to dynamically adapt and optimize performance. Figure 2.154 illustrates the current-voltage (*I-V*) and power-voltage (*P-V*) characteristics of the *PV* module, with the operating point (*OP*) dynamically tracked by the *MPPT* algorithm. The system consistently reached the *MPP* at point "A," even when the *OP* shifted due to load *R* or irradiance *G* changes. Load adjustments (e.g., *R*=450 Ω to 325Ω) caused oscillations around the *MPP*, while step changes in irradiance (1000 W/m^2 to 800 W/m^2) resulted in transitions between points (e.g., "*A*" to "*B*" and "*C*"). The system returned to the *MPP* (point "*A*") after each disturbance, with small oscillations in steady state, confirming the effectiveness of the *P&O* algorithm.

Figure 2.155 shows the duty cycle evolution driven by the *P&O* algorithm. When the irradiance and load remain constant, the duty cycle settles close to the expected value of 0.6. Figure 2.156 illustrates the changes in output voltage during the proposed scenario, confirming that the target DC output voltage of 120 V is maintained when the irradiance and load are adequate and stable.

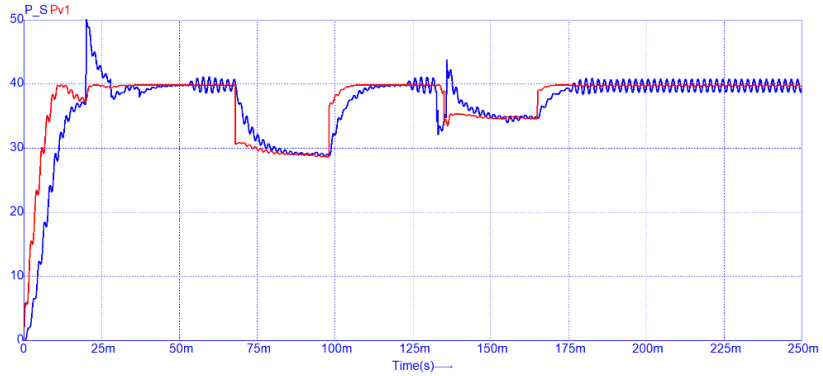

Figure 2.153 Simulation of input and output power during time according to the scenario.

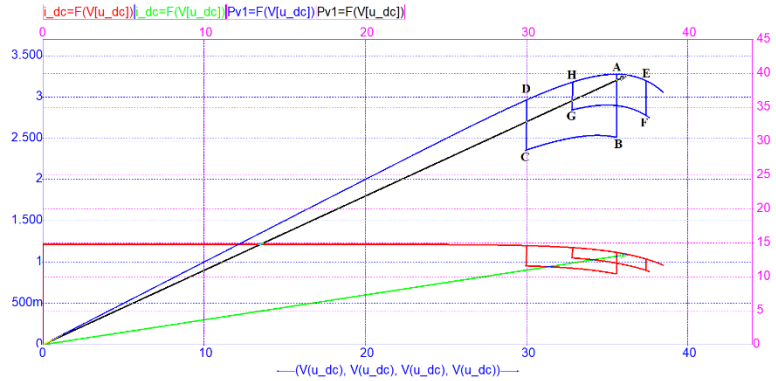

Figure 2.154 Simulation of the *OP* movement on the *I-V* and *P-V PV* module characteristics.

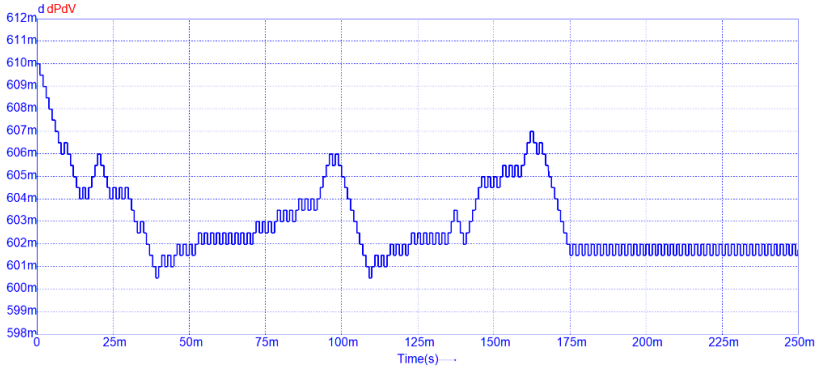

Figure 2.155 Duty cycle evolution against time for the proposed scenario

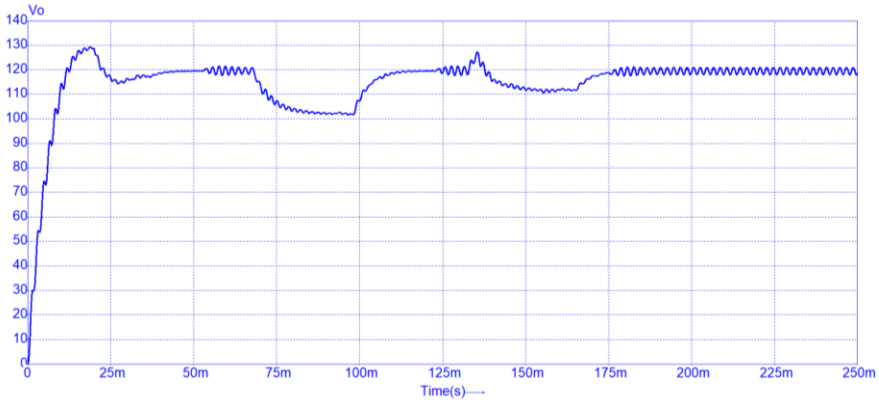

Figure 2.156 Output voltage against time during the proposed scenario.

A comprehensive analysis of Figure 2.153 to Figure 2.156, highlights the relationships between input and output power, current-voltage and power-voltage characteristics, duty cycle, and output voltage, demonstrating their evolution in response to changes over time.

The proposed converter, powered by two series-connected *PV* panels with the *P&O* algorithm for *MPPT*, was tested under varying conditions. A pyranometer [87] measured the solar irradiance and the *PV* temperature, with readings of G=885.6 W/m^2 and the corresponding V_{GPV} = 7.38 V, V_{TPV} = 8.24 V, and T_{PV} = 69.56 °C. Figure 2.157 shows the startup process, where the input voltage *Vin* initially equals the panels' open-circuit voltage 42 V and decreases to 35 V as the *MPP*

is reached after 5 seconds. The output voltage *Vout* reaches 110 V, with the *P&O* algorithm dynamically adjusting the duty cycle. Input current *Iin* and power *Pin* waveforms confirm that the algorithm maximizes power by increasing current as input voltage slightly decreases. Figure 2.158 captures the impact of shading a panel after 10.4 seconds, causing reductions in input voltage and power, while the *P&O* algorithm adjusts, demonstrating its robustness and effectiveness.

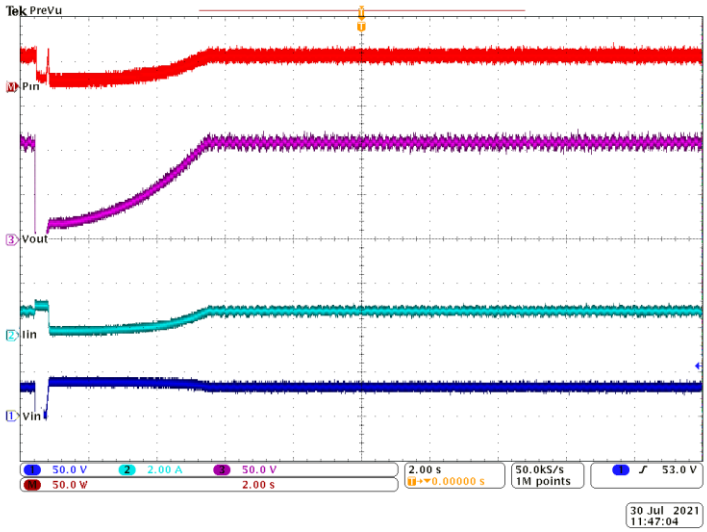

Figure 2.157 Oscilloscope waveforms at start-up for: input voltage *Vin*" (dark-blue), input current "*Iin*" (cyan), output voltage "*Vout*" (purple), and input power "*Pin*" (red), in down to up order.

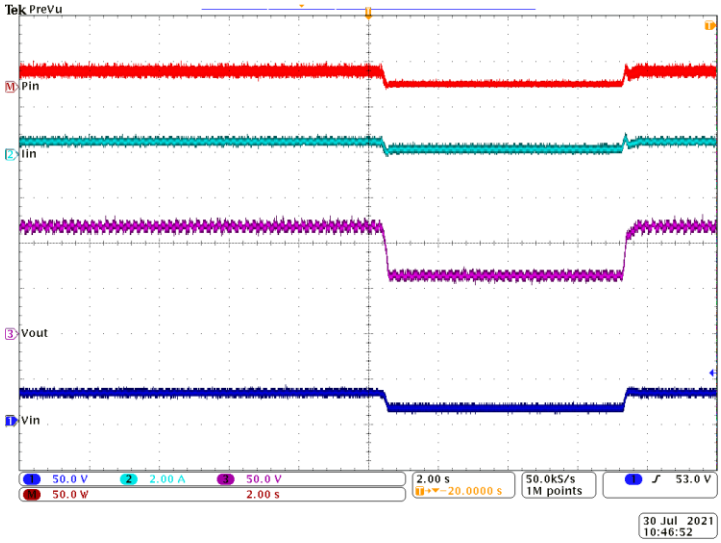

Figure 2.158 Oscilloscope waveforms for: input voltage "*Vin*"(dark-blue), output voltage "*Vout*"(purple), input current "*Iin*"(cyan) and input power "*Pin*"(red), in down to up order.

The system effectively uses the *P&O* algorithm to maintain the *MPP*, maximizing *PV* panel power. The converter advantages include a non-inverting output voltage and a non-floating transistor, simplifying control and enhancing performance. This work was supported by the grant of the Ministry of Research, Innovation and Digitization, CNCS/CCCDI—UEFISCDI, project number PD76/2020, within PNCDI III, [43].

2.1.4 Fuell cell applications

Fuel cell applications refer to the use of fuel cell technology to generate electricity through an electrochemical reaction between hydrogen and oxygen, [88]. Unlike combustion-based energy generation, fuel cells operate with higher efficiency, lower emissions, and higher reliability, [89], [90]. They are used in various industries for stationary, mobile, and portable power applications, [91]. With ongoing technological advancements and infrastructure development, fuel cells can become a mainstream energy solution, replacing fossil fuels in many applications. As green hydrogen production becomes more cost-effective, fuel cells could be widely adopted for zero-emission power generation, transportation, and industrial applications, contributing to a clean energy future, [92], [93].

Project SWARM is a European initiative focused on developing a fleet of hydrogen-powered small passenger vehicles while expanding hydrogen refuelling infrastructure across multiple regions to promote sustainable mobility, [94].

Jade University was responsible for integrating the fuel cell system into the electric drivetrain of the Elano e-mobiles and for optimizing their performance within the Project SWARM, [94]. To evaluate different control strategies, a test bench was developed that replicated real driving cycles for battery-fuel cell hybrid vehicles. Additionally, the compatibility of the lithium-iron phosphate battery with the Hydrogenics HyPM HD 8-200 fuel cell system while retaining the existing battery charger for range extension was ensured. A multiphase DC-DC converter was developed and tested under real vehicle drive cycle loads in the power electronics lab to improve drivetrain efficiency. Before full implementation, the drivetrain components on the test bench, followed by their integration into two prototype vehicles for further optimization were tested and validated. The author contributed to the development, testing, and optimization of fuel cell powertrain systems, focusing on improving energy efficiency and integrating innovative technologies into hybrid vehicles and this research findings have been materialized in several subsequent papers.

2.1.4.1 A new concept for powertrain control in battery fuel cell hybrid vehicles

An innovative approach for controlling the drivetrain in battery fuel cell hybrid vehicles by replacing the conventional DC-DC converter with a simplified power electronic switch is presented in [39]. This switch operates in a linear mode during switch-on and switch-off phases, ensuring smooth power transfer. To handle the high switching loads, multiple semiconductors are connected in parallel, with their individual currents continuously monitored and balanced by a microprocessor-based control circuit. The study concludes with the practical implementation of this power electronic switch in a test bench, demonstrating its effectiveness in replicating real-world drivetrain operation for battery-fuel cell hybrid vehicles.

Drive train of fuel cell vehicles

A fuel cell system alone cannot provide sufficient power for the varying demands of vehicle drive cycles. Therefore, an energy storage unit, typically a battery, must be connected in parallel with the fuel cell system to ensure stable power delivery. Alternatively, double-layer capacitors can be used as storage components. Traditionally, a DC-DC converter is employed to interconnect the fuel cell and energy storage, optimizing power distribution between the two sources. Figure

2.159 illustrates the typical electrical drivetrain configurations of both battery-electric vehicles and battery-fuel cell hybrid vehicles.

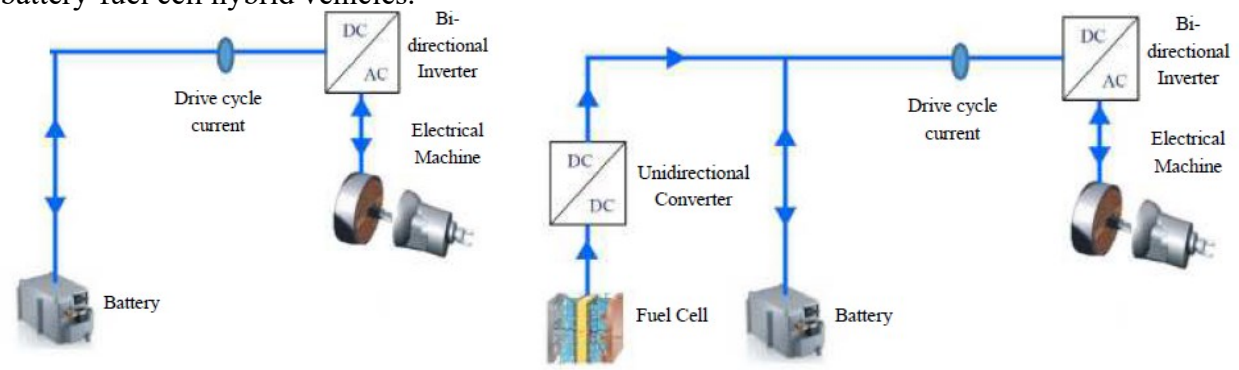

Figure 2.159 Typical drive train of a battery electric - (left) and a battery fuel cell hybrid vehicle (right).

Following the modification of Elano e-mobiles into elanoFC vehicles, the existing battery will remain an integral part of the drivetrain. Additionally, the built-in battery charger will be retained to enable the fuel cell system to operate as a range extender. Instead of using a conventional DC-DC converter, the proposed system will incorporate a power electronic switch. This switch will allow the direct interconnection of the battery and the fuel cell system when required, simplifying the powertrain design while maintaining efficient energy management. Drive train with electronic switch circuit (left) and the behaviour of the fuel cell system (right) is shown in Figure 2.160.

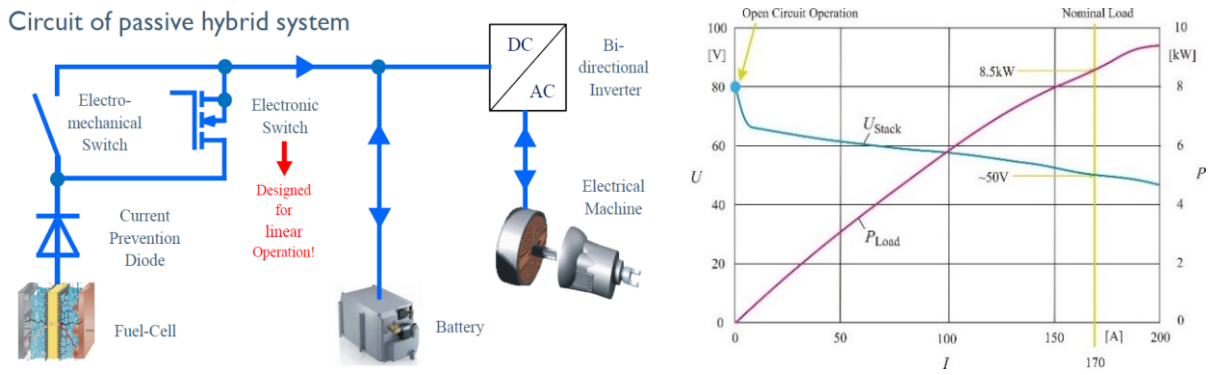

Figure 2.160 Drive train with electronic switch circuit (left) and the behaviour of the fuel cell system (right).

The passive hybrid system synchronizes the switching process and hydrogen supply with the fuel cell power changes to prevent operational issues. The electronic power switch operates in a linear mode for several seconds, ensuring smooth transitions. Voltage matching between the fuel cell (Hydrogenics HYDM HD8-200, 8.5 kW, 80V open-circuit voltage) and the battery is essential for ensuring stability.

In the drivetrain, the drive inverter and the electric machine are directly connected to the battery, while a diode at the fuel cell output prevents reverse energy flow. The electronic switch gradually connects the fuel cell to the battery, automatically stabilizing operation. A mechanical switch could further reduce energy losses, but it is unnecessary in this design.

The linear operation of the power electronic switch leads to high power losses during extended switching periods, exposing the semiconductors to significant stress for several seconds.

To ensure safe operation, six MOSFETs are connected in parallel, with their individual currents monitored and regulated by a microprocessor circuit.
As shown in Figure 2.161, switch-on tests indicate a switching duration of approximately 25 seconds, with an initial switch voltage of 22V. These tests remain part of the development phase, and measurements cease after the switch-on process is completed.

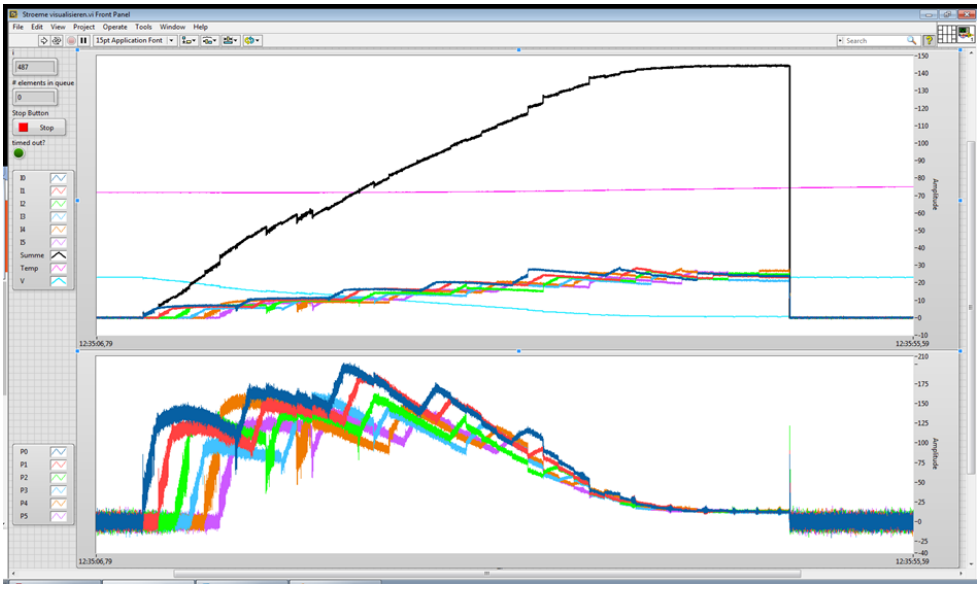

Figure 2.161 Current (above) and power losses (below) in the MOSFETs during switching operation.

The current waveforms in the MOSFETs during the switch-on process show a stepwise increase in current across the six MOSFETs. The total switch current (I_{Switch}) is the sum of the individual MOSFET currents. During switching, the voltage across the electronic switch gradually decreases to the forward voltage level, while the heatsink temperature remains stable.

The power loss curves, derived from current waveforms and voltage measurements, indicate maximum losses of nearly 200W per MOSFET module. By employing a step-by-step switching approach, the total power losses are effectively distributed among the MOSFETs, preventing excessive thermal stress on individual components. The electronic switch implementation, shown in Figure 2.162, uses IXTN200N10L2 MOSFETs designed for linear operation. The microprocessor continuously measures and balances currents across the six MOSFET modules. For verification, measured currents can be accessed via BNC sockets. A thermographic image confirms that after multiple switching operations, the temperatures remain within safe limits, ensuring stable performance.

The current gradient and switching time are controlled via CAN communication, with the microprocessor automatically setting the current level based on the battery's state of charge.
As shown in Figure 2.163, in the left example, the current increases to 115A in 8.4s, while in the right example, the current stabilizes at 210A, with both switch-on and switch-off durations of 5s.

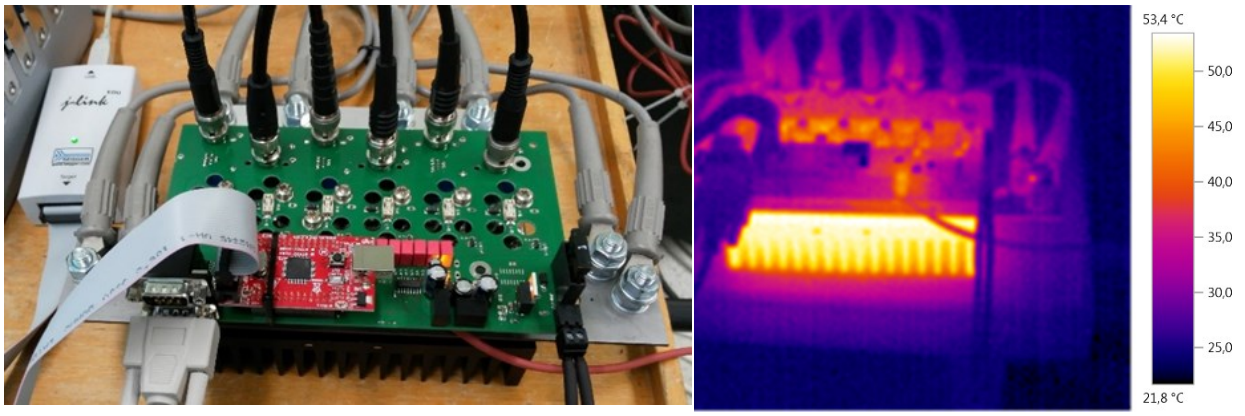

Figure 2.162 Electronic switch (left) with a temperature profile after same switching operations (right).

Figure 2.163 Different current waveforms during switching operations with the electronic switch.

Test bench for the drive train of battery-fuel cell hybrid vehicles

The drivetrain of an electric vehicle consists of an electric machine powered by an inverter, with a battery in the DC-link circuit (Figure 2.159 left). During engine operation, the battery supplies energy, while in braking or deceleration, the machine acts as a generator, feeding energy back into the battery.

At the test bench, the electric machine is replaced by power supplies and electronic loads, capable of handling discharge currents up to 420A and charging currents up to 260A. A LabVIEW program controls these components to accurately replicate real drive cycles. Figure 2.164 illustrates the passive hybrid system setup, with a 10-minute segment of a recorded drive cycle shown on the right.

The test bench, shown in Figure 2.165, integrates a fuel cell system, lithium-iron-phosphate battery, power supplies, and electronic loads to evaluate the power electronic switch under real driving conditions. The fuel cell system must operate within its permissible range throughout the test cycle.

Key components include thin gas pipes that supply hydrogen from an external bottle, while ambient air is compressed by a blower to enable the hydrogen-oxygen reaction within the fuel cell. A cooling circuit, featuring a motorbike cooler, is used for heat dissipation to maintain stable operation.

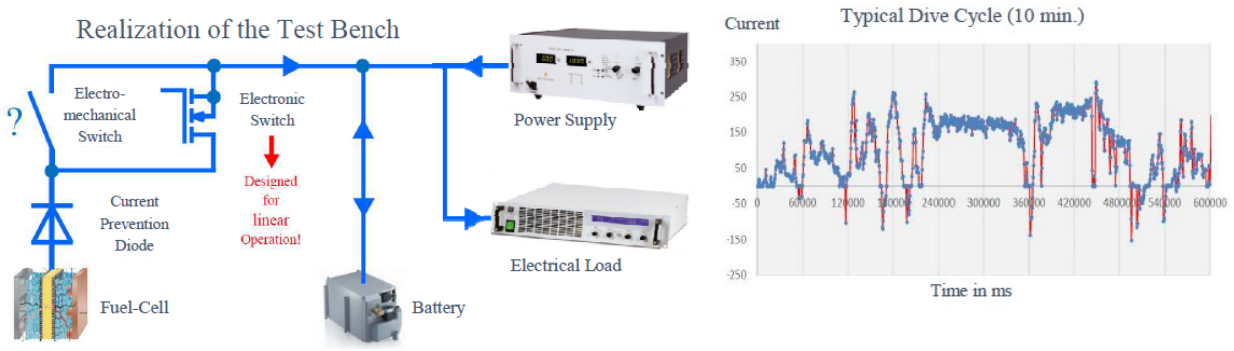

Figure 2.164 Overview of the test bench (left) and the current waveform during a drive cycle (right).

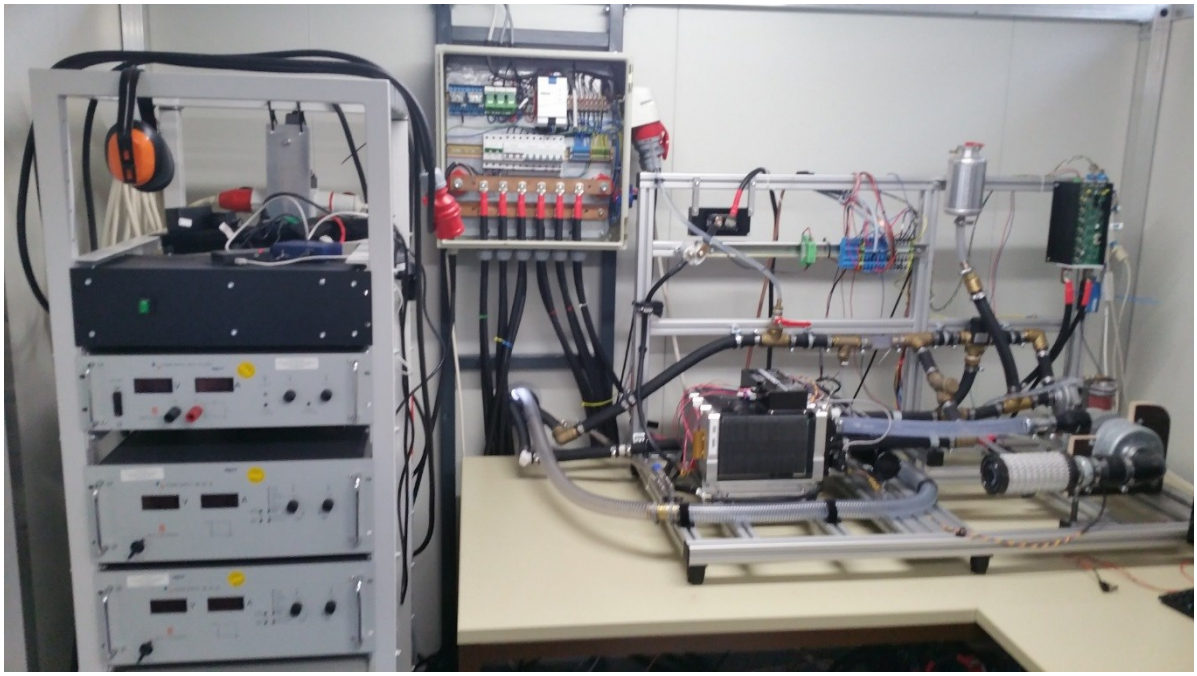

Figure 2.165 Realization of the test bench to control the drive train of battery-fuel cell hybrid vehicles [3].

Practical measurements in the test bench

In battery-fuel cell hybrid vehicles, the electronic switch establishes an automatic operating point when switched on. However, during drive train load cycles, battery voltage fluctuations cause variations in both current and power output of the fuel cell system.

To analyse this behaviour, initial measurements are conducted in switched-*on* state using variable electronic loads, replicating only the engine drive cycle. The 15-minute measurement results are shown in Figure 2.166, where the battery current (yellow), fuel cell current (red), and maximum allowed fuel cell current (blue) are displayed.

The drive cycle current primarily affects the battery, that discharges when the current is negative and charges when it is positive. The fuel cell current remains largely DC, with minor variations corresponding to the load cycle. The load current is determined by the difference between the battery and fuel cell currents.

The fuel cell system power must be coordinated with the hydrogen supply, which sets a maximum allowable current. In Figure 2.166, the allowed fuel cell current (blue) consistently exceeds the actual current (red), ensuring safe operation.

Figure 2.167 shows that the battery voltage (purple) and fuel cell voltage (green) remain roughly constant, with the fuel cell voltage slightly higher due to the positive fuel cell current. In Figure 2.168 and Figure 2.169, a 17-minute test demonstrates that the fuel cell system activates at 15% battery state of charge and shuts down at 16%, confirming effective control of the powertrain.

In Figure 2.168, the fuel cell system starts operating at 15% battery state of charge, splitting the drive cycle current between the fuel cell and battery, allowing slow charging. After a few minutes, the fuel cell shuts down, and the cycle repeats. An initial overshoot in fuel cell current is followed by a brief undershoot, but this is not considered critical by the manufacturer.

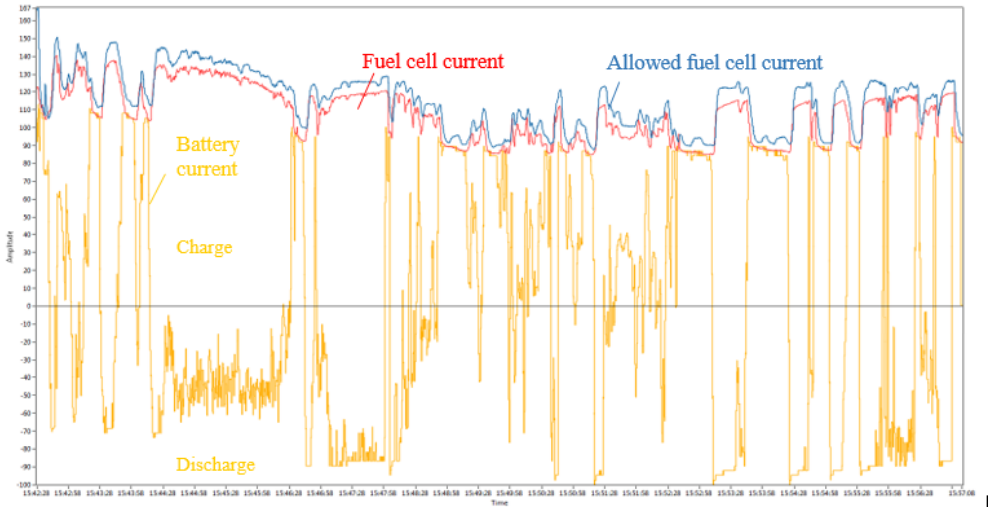

Figure 2.166 Battery (yellow), fuel cell (red) and allowed fuel cell current (blue) during a drive load.

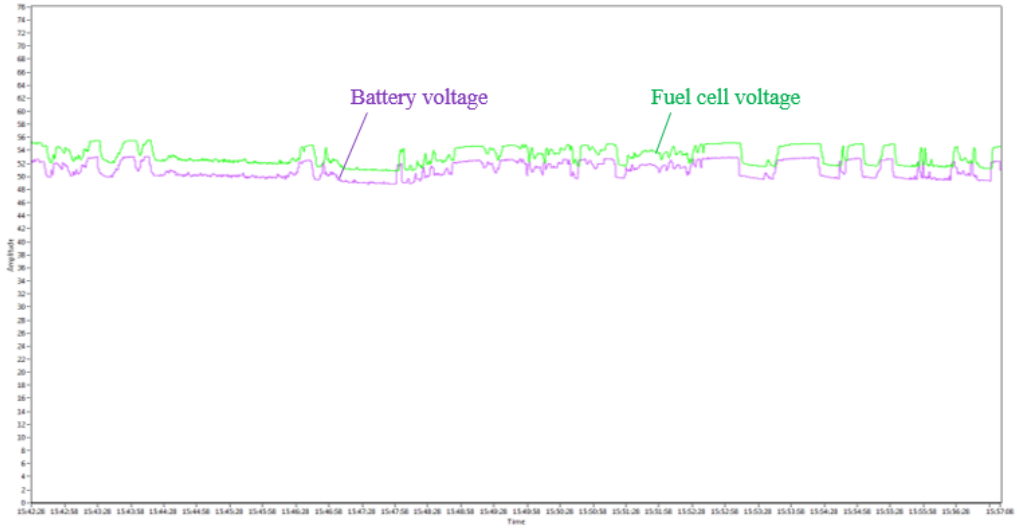

Figure 2.167 Battery voltage (purple) and the fuel cell voltage (green) during a drive load.

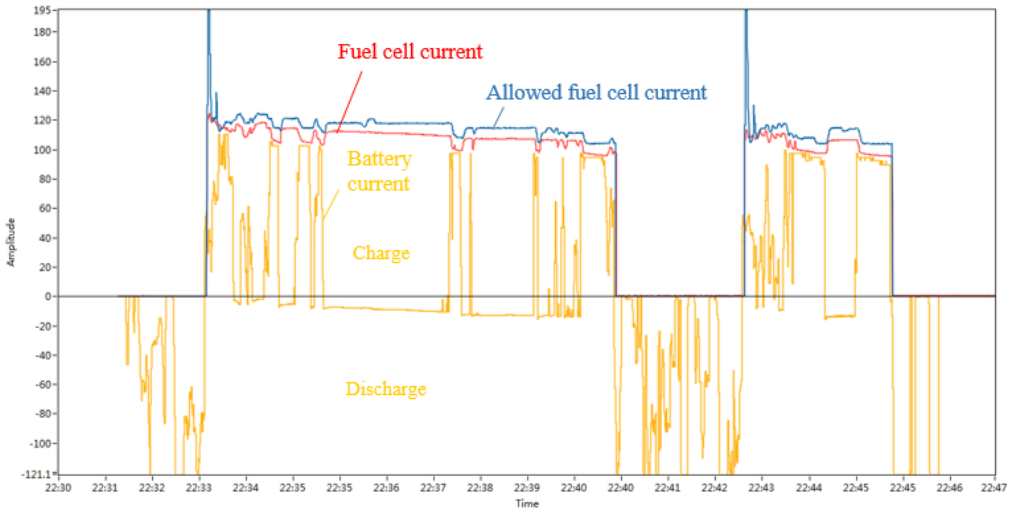

Figure 2.168 Battery (yellow), fuel cell (red) and allowed fuel cell current (blue) during a drive load.

Figure 2.169 shows that battery and fuel cell voltages remain stable. When the fuel cell starts, its voltage rises close to the open-circuit voltage, then settles slightly above the battery voltage due to voltage drops in power lines and components. When the switch turns off, the fuel cell voltage returns to open-circuit level before shutdown.

A vehicle management system will control the switching points, factoring in battery charge, hydrogen supply, system load, and temperature. The operating strategy will be tested on the bench before vehicle implementation, enabling step-by-step drivetrain optimization.

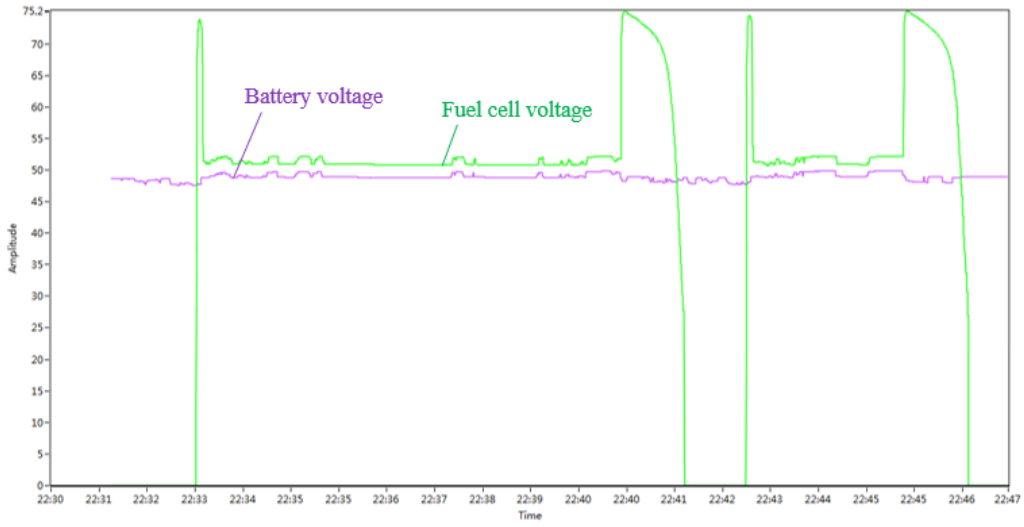

Figure 2.169 Battery voltage (purple) and the fuel cell voltage (green) during a drive load.

The proposed electronic switch-based powertrain control simplifies the drivetrain of battery fuel cell hybrid vehicles, ensuring efficient power distribution through MOSFET-based current balancing. Successfully tested under real driving conditions, it will be further optimized and integrated into vehicle management systems at Jade University.

2.1.4.2 Test bench to optimize the powertrain in battery-electric and fuel-cell vehicles

A test bench was designed and practically implemented to replicate the measured cyclic current profiles of electric vehicle powertrains. The system was developed to enable accurate simulation of real-world operating conditions by incorporating advanced hardware and software features. The test bench facilitates the acquisition and storage of measurement data at defined time intervals, allowing for comprehensive evaluation and analysis. Additionally, it includes mechanisms to monitor operational parameters and manage limit exceedances to ensure testing reliability and safety. Experimental results from long-term testing of single battery cells demonstrate the test bench capability to simulate powertrain loads under realistic conditions. Furthermore, the system has been extended to reproduce the powertrains of both battery-electric and fuel-cell vehicles, contributing to the advancement of energy storage and power management technologies in the automotive sector, [40].

The development of powertrains for battery-electric and fuel-cell vehicles has been extensively studied in the literature, with comparisons addressing aspects such as cost, volume, mass, and fuel economy. Typically, the drivetrain of a battery-electric vehicle consists of an electric machine controlled by an inverter, Figure 2.159, complemented by a battery storage system to store and supply energy. During operation, energy is drawn from the battery for propulsion, while regenerative braking allows energy to be fed back into the battery, [95], [96], [97], [98], [99] and [100].

For the test bench implementation, the electric machine is replaced by power supplies and electronic loads, allowing the system to replicate acceleration phases via electronic loads and braking or deceleration phases using power supply units, Figure 2.170. The current test bench is the same like the previous one from the last section, capable of handling discharge currents up to 420A and charging currents up to 260A, with the possibility of extending power capacity through the parallel connection of multiple equipment units. This setup provides a realistic testing environment for evaluating powertrain performance and optimizing energy management strategies in electric and fuel-cell vehicle systems.

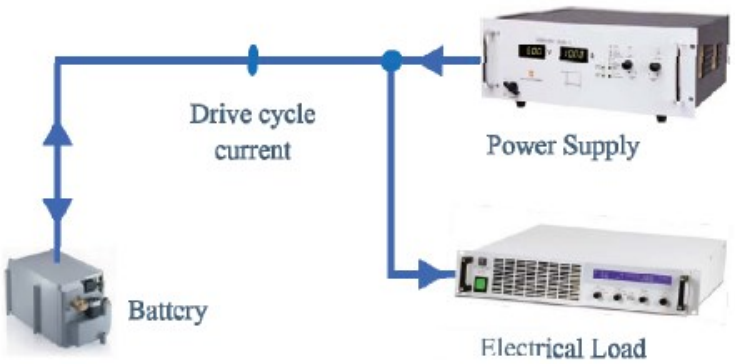

Figure 2.170 Drive train of an electric vehicle with machine fictive load.

To replicate a complete drive cycle, LabVIEW software controls the electronic loads and the power supplies, enabling precise reproduction of measured drivetrain currents. The system records current and voltage on the Device Under Test (DUT) every 100ms for detailed evaluation.

The test bench uses modular power supplies from Elektro-Automatik GmbH, supporting constant current and voltage regulation. These units have fast response times (5ms) and can be

expanded via a master-slave function. Electronic loads allow high-current testing at low voltages 0.7V. With rapid response times 50µs, even smaller current rise and fall times are possible with electronic loads, making them ideal for individual battery cell testing.

The power supplies and electronic loads support various interface cards for control by a computer. For the battery test bench, a USB interface card type IF-U1 is used, and automatically shuts down if the voltage limits on the DUT is above or below the previously entered limit value for a half a second, sending email alerts and allowing remote diagnostics via smartphone, Figure 2.171. A main contactor (Albright SW200 48V) ensures emergency disconnection, and an emergency stop switch allows manual shutdown.

For hardware safety, temperature and voltage are continuously monitored, with automatic shutdown if limits are exceeded. An uninterruptible power supply (*UPS*) prevents uncontrolled shutdowns during endurance testing, ensuring reliable and safe operation of the test bench for battery-electric and fuel-cell powertrain evaluations., Figure 2.172.

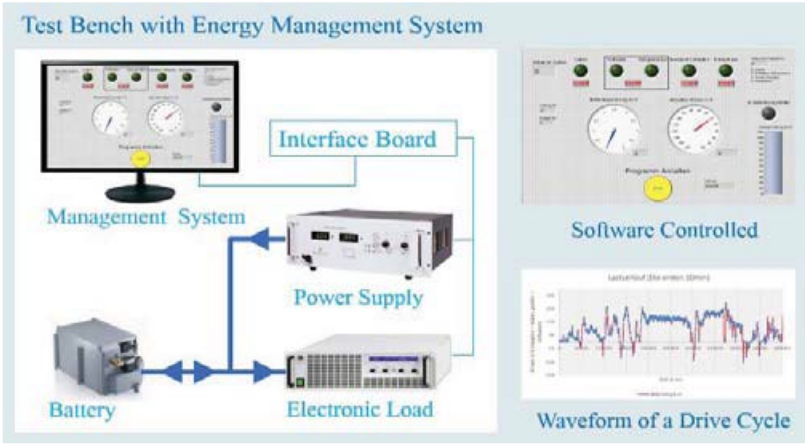

Figure 2.171 Software controlled test bench with a power management system.

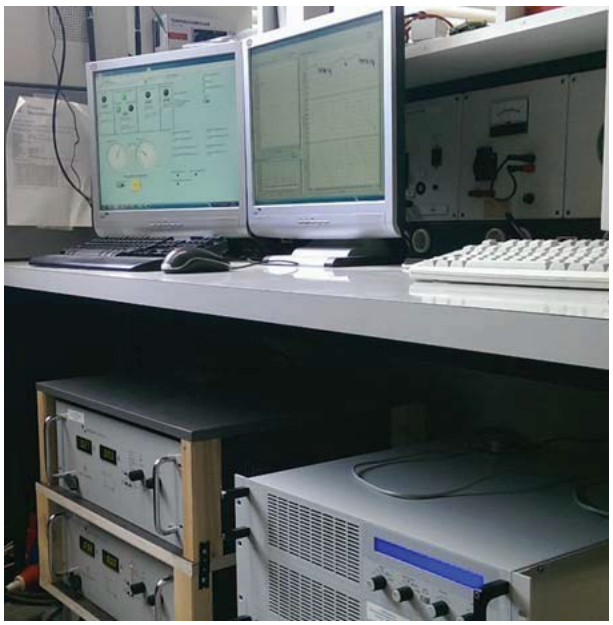

Figure 2.172 Practical realization of the software-controlled test bench [101].

The test bench was used to evaluate lithium iron phosphate (LiFePO4) battery cells by applying a recorded 160-minute current profile from an electric vehicle drive cycle. Figure 2.173 shows a 10-minute segment of this profile. Testing involved cyclic charging and discharging, following a constant current/constant voltage (*IU*) method with predefined voltage limits, and included resting phases to assess battery capacity.
The initial test on Winston WB-LYP100AHA cells used a charge voltage of 3.65V, a discharge voltage of 2.8V, and a maximum current of 100A. Results indicated rapid aging, with a steep voltage rise at the end of each charge cycle (Figure 2.174). To improve longevity, a second test reduced the charge voltage to 3.45V, increased the discharge voltage to 2.9V, and limited charging/discharging to 50A.

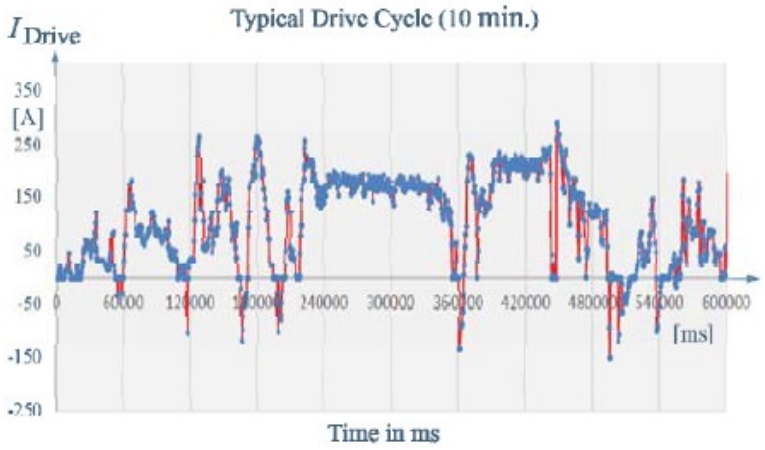

Figure 2.173 Time segment from the recorded drive cycle [101].

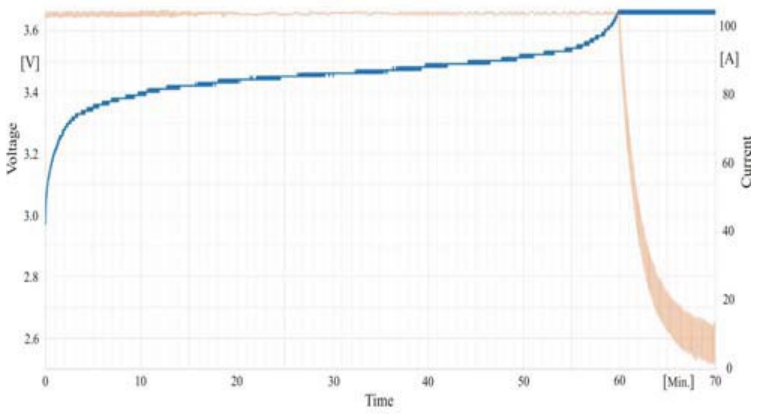

Figure 2.174 Voltage and current waveform at the IU charge of a battery cell [101].

Over 5 months and 680 cycles, efficiency remained stable at 92.5%, with minimal energy loss (Figure 2.175). The first battery cell reached end-of-life after 321 cycles, while the second cell retained 100% of its rated capacity, aligning with manufacturer specifications, predicting 80% retention after 3000 cycles.

The test bench can be also evaluate entire battery systems, including battery management system (*BMS*) balancing circuits, and can be extended to test power distribution in fuel cell hybrid vehicles, enabling comprehensive powertrain testing, Figure 2.176.

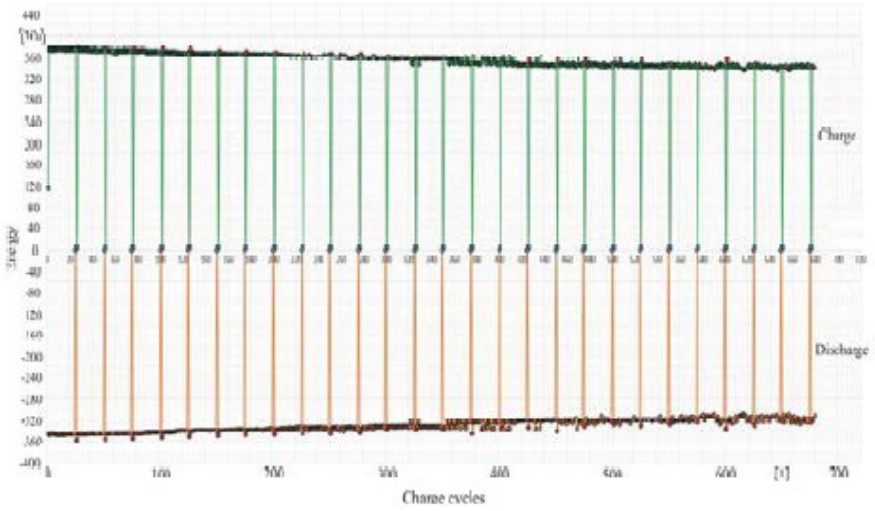

Figure 2.175 Supplied or dissipated energy as a function of cycle numbers [101].

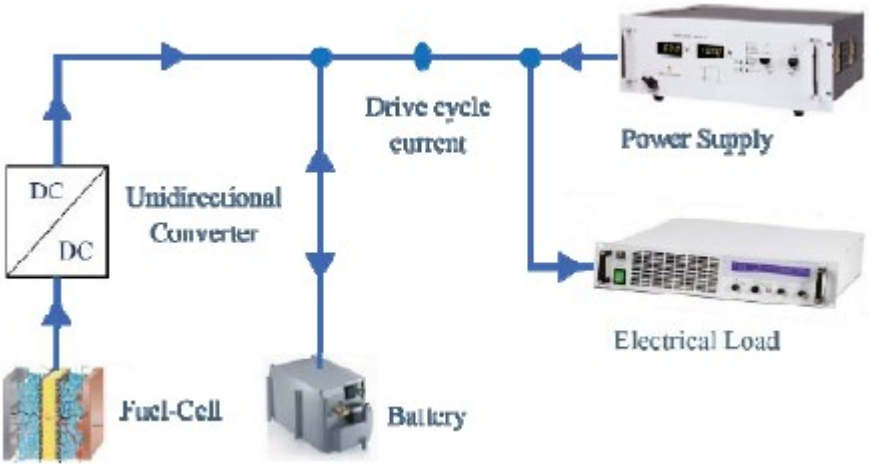

Figure 2.176 Powertrain of a fuel cell vehicle [102]- [103].

Beyond battery life testing, the test bench can simulate complete powertrain operation for both battery-electric and fuel-cell vehicles. This capability allows for optimization of vehicle operation strategies, ensuring efficient energy management and prolonging component lifespan in the drivetrain. By replicating real-world power demands, the system helps refine control algorithms and assess the durability of critical components, contributing to the development of more reliable and long-lasting powertrain solutions.

2.1.4.3 Multiphase DC/DC converter and its use in the powertrain of fuel cell vehicles

The Elano e-mobile fuel cell vehicle retains its lithium iron phosphate battery with a rated energy of 10 kWh and a voltage of 50V. A Hydrogenics HyPM HD 8-200 PN fuel cell system is integrated as a range extender, delivering 8.5 kW, with an open circuit voltage of 80V. To maintain charging capabilities, the existing onboard battery charger remains in use. A multiphase DC-DC converter is developed to optimize energy transfer and tested under real drive conditions, enabling drivetrain optimization through improved control strategies, [41].

Theoretical analysis

For this application a synchronous buck converter is selected for voltage step-down operations. A multiphase topology is adopted to distribute load currents among several phases, reducing the stress on individual components, Figure 2.177. The interleaved PWM technique is employed to phase-shift switching signals, effectively reducing current ripple and improving efficiency, Figure 2.178. Analytical expressions for inductor and capacitor selection in multiphase configurations are derived and presented in [102] and in [41].

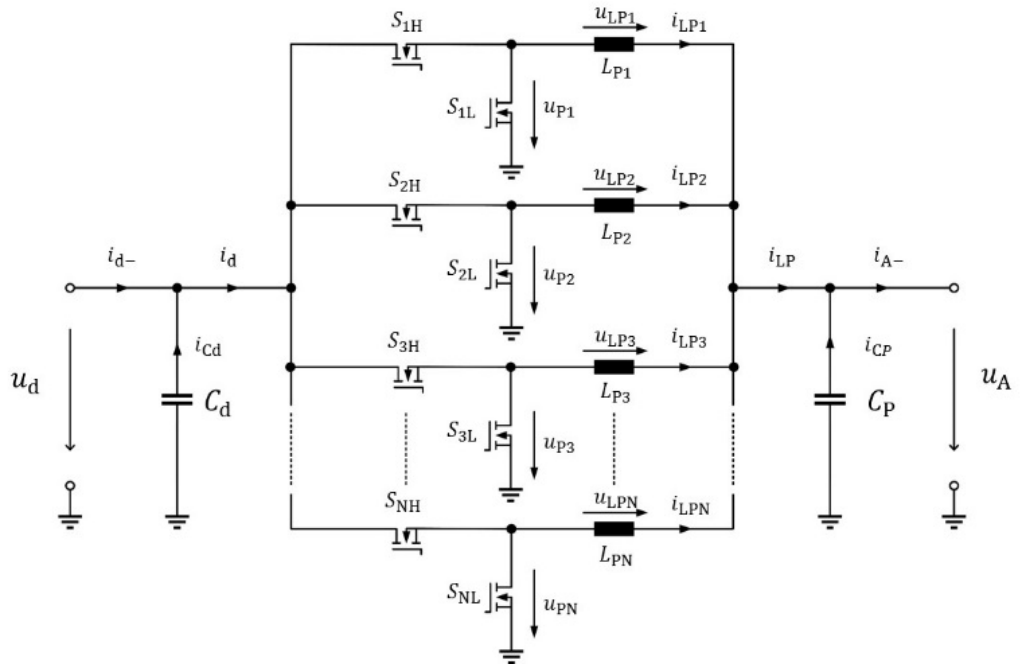

Figure 2.177 Power part of a multiphase DC-DC converter [102]

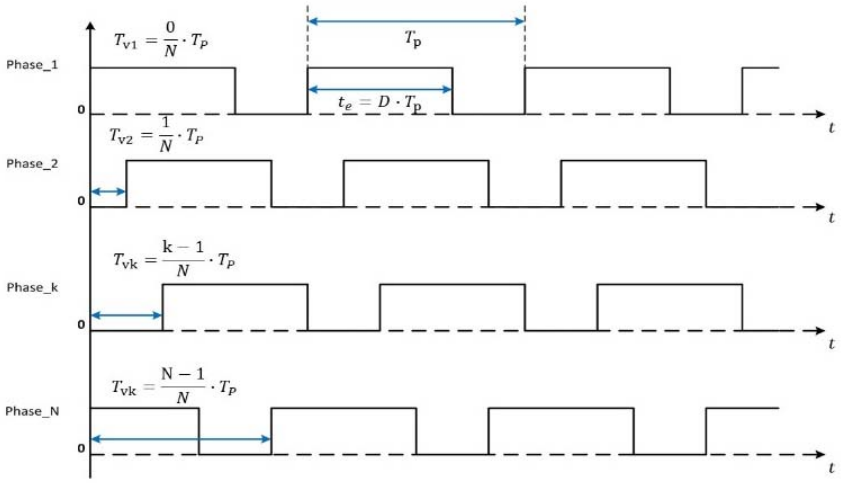

Figure 2.178 PWM signals for different converter phases [102].

Practical Implementation

A six-phase buck converter (8.5 kW) is developed to regulate energy exchange between the fuel cell system (55-80V) and the lithium iron phosphate battery (45-55V), Figure 2.179. The converter power board (30cm × 20cm × 12cm) integrates half-bridges, gate drivers, and copper bars to handle currents up to 180A. A filter circuit board with 3D-printed inductor coils and current sensors ensures balanced phase loads. The control system is implemented using an STM32-based NUCLEO-F767ZI microcontroller, which generates interleaved PWM signals at 26.67 kHz, controlling phase synchronization, Figure 2.180. Figure 2.181 illustrates inductor currents for phase 1 and phase 4. Initially, unbalanced currents arise due to component tolerances and PWM signal deviations, risking component overload. The balancing control circuit adjusts PWM signals, ensuring equal *DC*-current values, improving system stability and reliability. A balancing controller adjusts *PWM* signals to equalize inductor currents, preventing component overload, Figure 2.182.

Efficiency measurements confirm 95-98% performance, particularly effective at 60V to 50V conversion, optimizing fuel cell vehicle powertrain efficiency under varying load conditions, Figure 2.183.

Figure 2.179 Power part of the converter with gate-driver circuits [102].

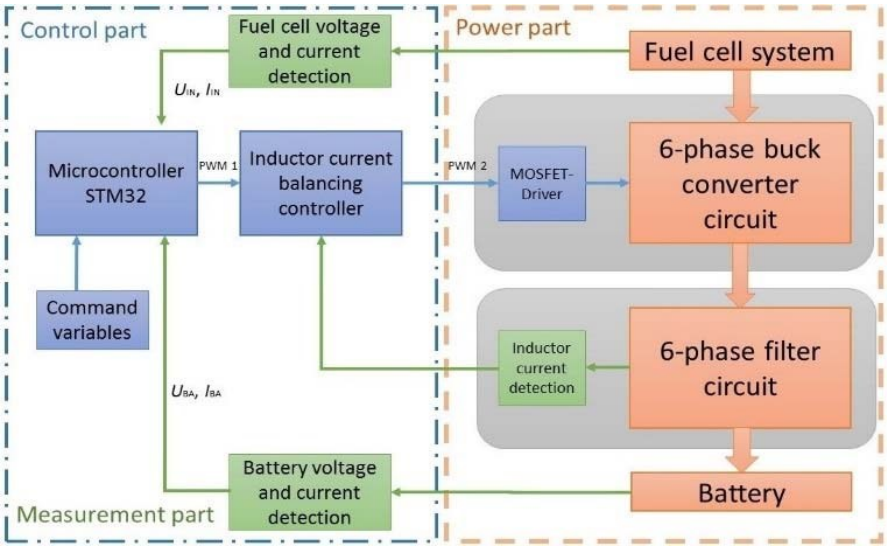

Figure 2.180 Control block of the multi-phase DC-DC converter [102].

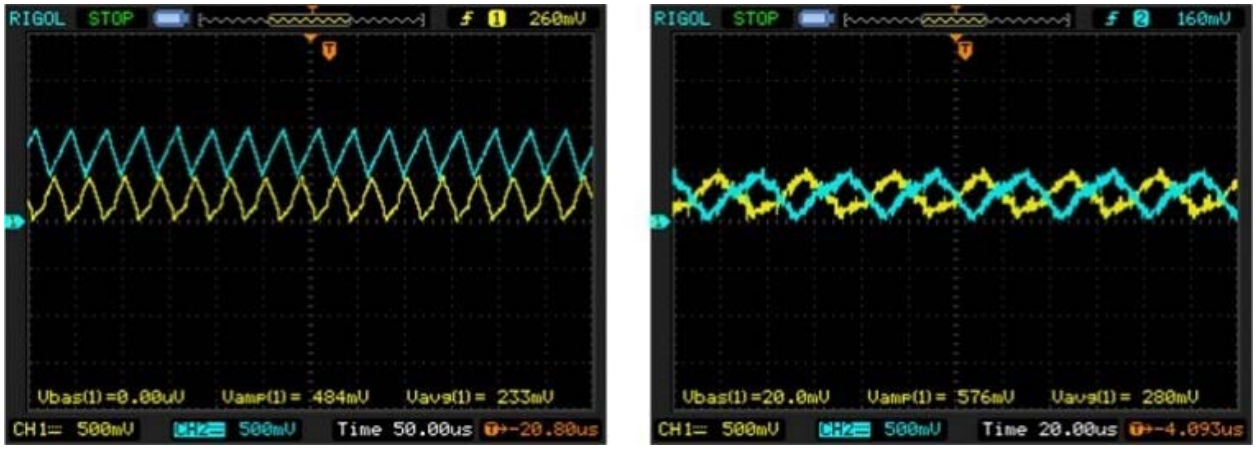

Figure 2.181 Inductor currents without (left) and with the control circuit (right).

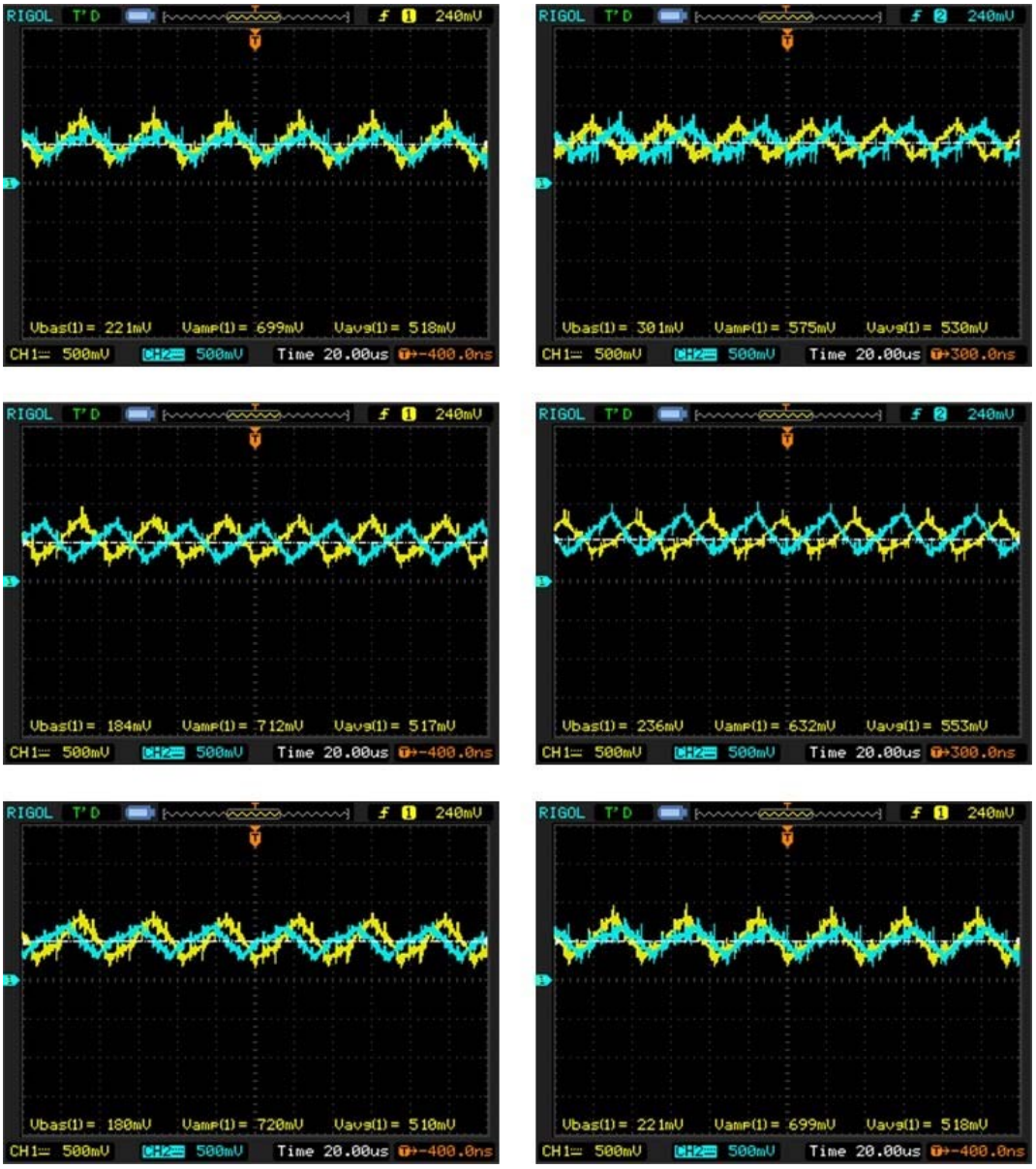

Figure 2.182 Inductor currents in the different phases with the balancing circuit.

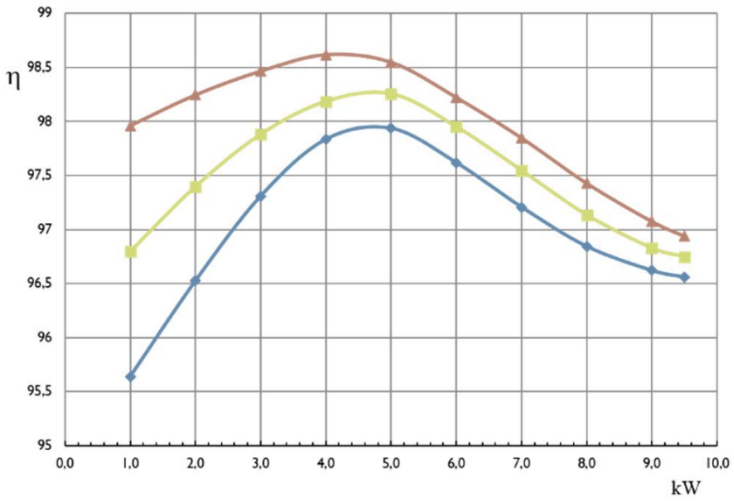

Figure 2.183 Efficiency diagram against power for the multi-phase DC-DC converter.

Using the reproduction of the powertrain for fuel cell vehicles and the software controlled test bench with power management system implemented in [40], a test bench that replicates real-world driving scenarios by simulating acceleration, deceleration, and regenerative braking is implemented and shown in Figure 2.184. The test bench allows evaluation of various DC-DC converter operation strategies. It can function as a range extender with constant load or adjust power based on battery state of charge, increasing its output as the battery discharges. At low power levels, some converter phases can be deactivated to enhance efficiency.

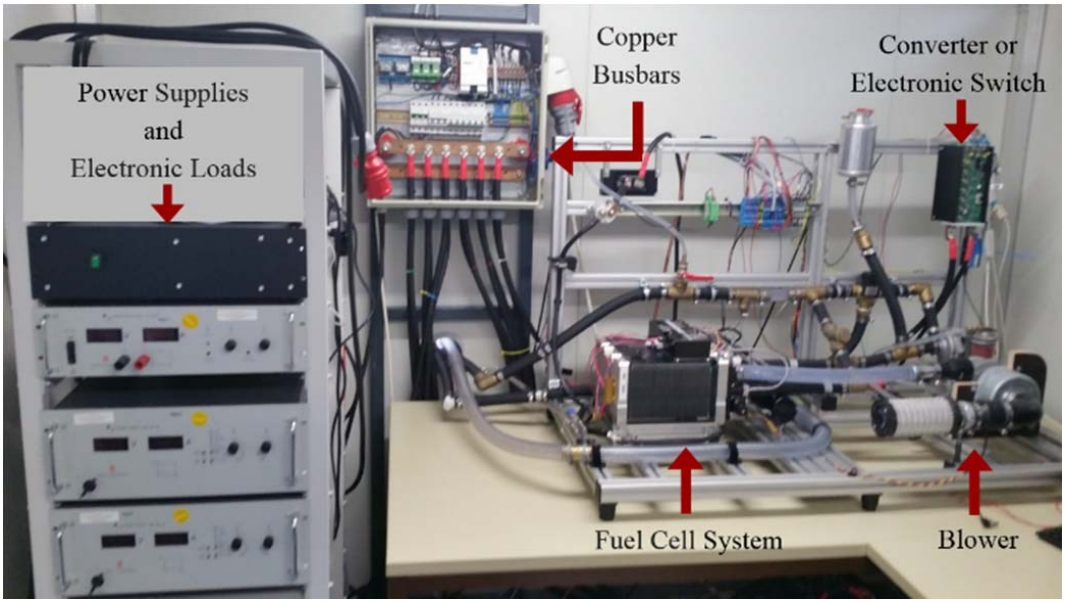

Figure 2.184 Test bench for reproducing the drive train of fuel cell vehicle.

For real driving conditions, a vehicle management system dynamically adjusts the converter operation based on battery charge, hydrogen supply, electrical loads, and temperature. Strategies are tested on the bench before vehicle implementation, ensuring step-by-step powertrain

optimization. The control strategy optimizes power distribution between the fuel cell and the battery, extending component lifespan and improving vehicle performance.

2.1.4.4 Control strategy for a DC/DC converter in drive train of fuel cell vehicles

Fuel cell vehicles exhibit dynamic operational conditions due to frequent acceleration, deceleration, and regenerative braking. The fuel cell system, however, has a inherent slow response and therefore it requires the integration of an auxiliary energy storage device such as a battery or supercapacitor. To optimize power flow and system stability, different configurations of the fuel cell hybrid drive train have been analysed, [38]. Each configuration employs a distinct power conversion approach to balance the power demand between the fuel cell system and the energy storage device.

The first configuration, Configuration I, Figure 2.185, incorporates a bidirectional DC-DC converter between the DC bus and the battery. This design enables energy exchange between the fuel cell system and the battery, allowing efficient power distribution during varying load conditions.

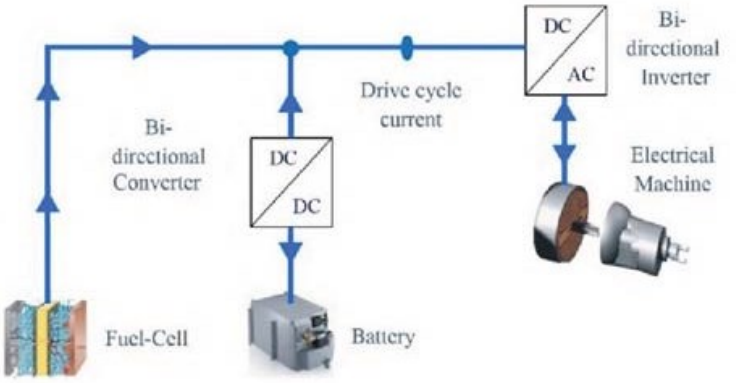

Figure 2.185 Configuration I of the hybrid drive train in fuel cell vehicle.

In Configuration II, Figure 2.186, a unidirectional DC-DC converter is placed between the fuel cell system and the DC bus. This setup directly controls the fuel cell power output, ensuring stable operation by compensating for its slow response to sudden load variations.

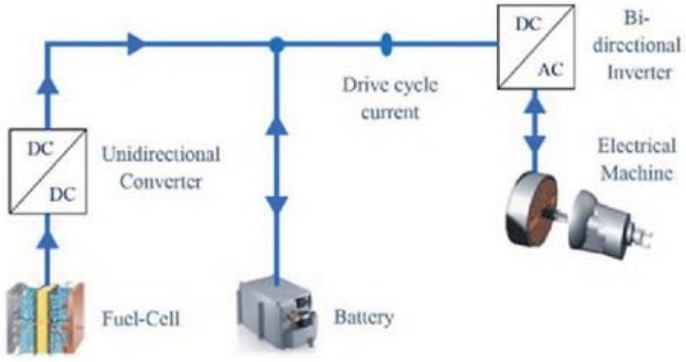

Figure 2.186 Configuration II of the hybrid drive train in fuel cell vehicle.

The third configuration, Configuration III, Figure 2.187, eliminates the DC-DC converter, replacing it with a power electronic switch. This approach allows direct interconnection between the fuel cell system and the battery, simplifying the powertrain architecture while still facilitating energy management.

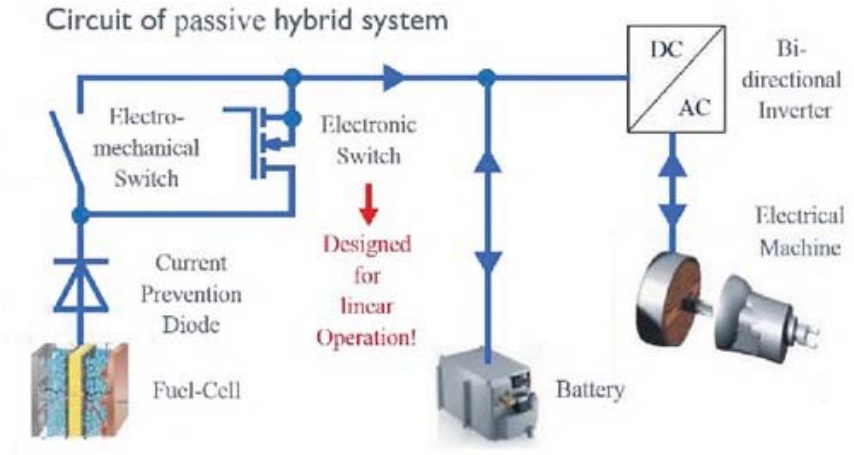

Figure 2.187 Configuration III of the hybrid drive train in fuel cell vehicle.

Each configuration has unique advantages and challenges, influencing factors such as system efficiency, response time, and component complexity. The paper evaluates these configurations to determine the most effective strategy for integrating fuel cells into electric vehicle powertrains, [38].

In a passive hybrid system, the fuel cell system (Hydrogenics HYDM HD8-200, 8.5 kW, 80V open circuit voltage) and battery must have compatible voltages. Figure 2.188 shows that fuel cell voltage drops rapidly under load, stabilizing as current increases. At nominal power (170A), the output voltage reaches 50V, which must align with the battery fully discharged state.

During operation, DC bus voltage fluctuates based on battery charge level and power demands of the electrical machine controller. Consequently, the fuel cell operating point shifts along its U-I curve, particularly in the purple region of the graph, affecting overall system efficiency.

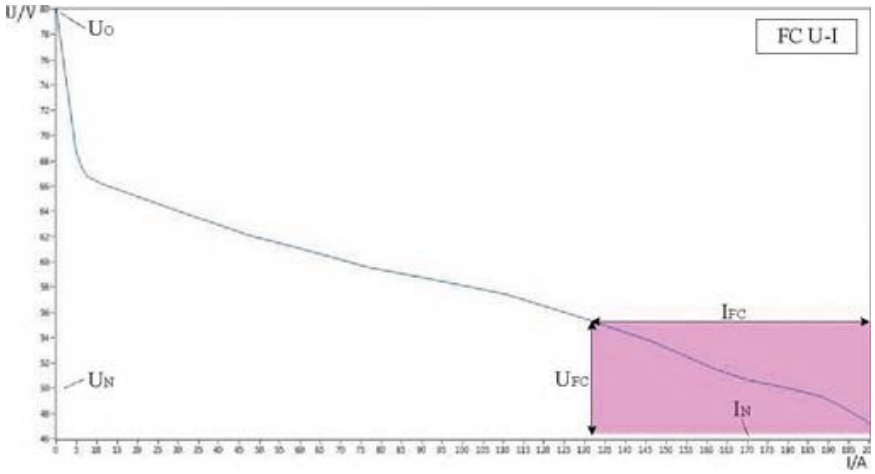

Figure 2.188 The output behaviour U-I curve of the fuel cell system.

Fuel cells operate most efficiently in a stable operating point, but their slow response to load changes and mechanically controlled fuel supply reduces efficiency and shortens lifespan. Additionally, fuel cell output characteristics are inherently soft (as shown in Figure 2.188), leading to inefficiencies when responding to dynamic power demands.

A DC-DC converter is essential in the drivetrain to actively regulate fuel cell operation, ensuring optimal efficiency and longevity. To simplify analysis, the fuel cell drivetrain is modelled as a two-port network (Figure 2.189), where the battery and motor controller are combined into a single load (R_L). This load, along with the DC-DC converter, represents the equivalent input impedance (R_{Eq}) seen by the fuel cell system.

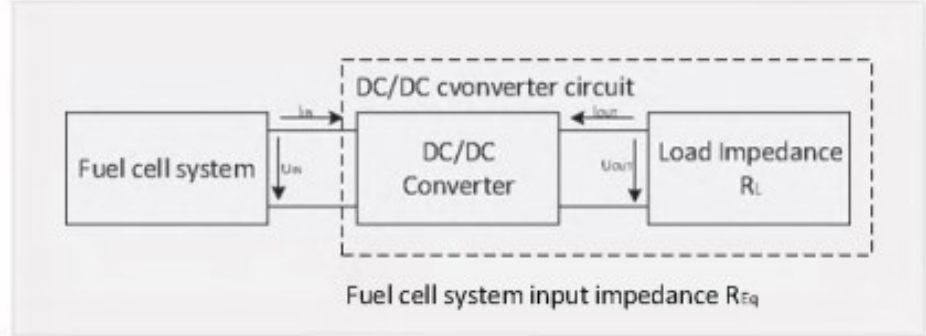

Figure 2.189 Two-port network of fuel cell hybrid drive train (Configuration II).

Figure 2.190, illustrates the relationship between the amplification factor—defined as the ratio of equivalent input impedance R_{Eq} to load impedance R and the duty cycle D of the DC-DC converter.

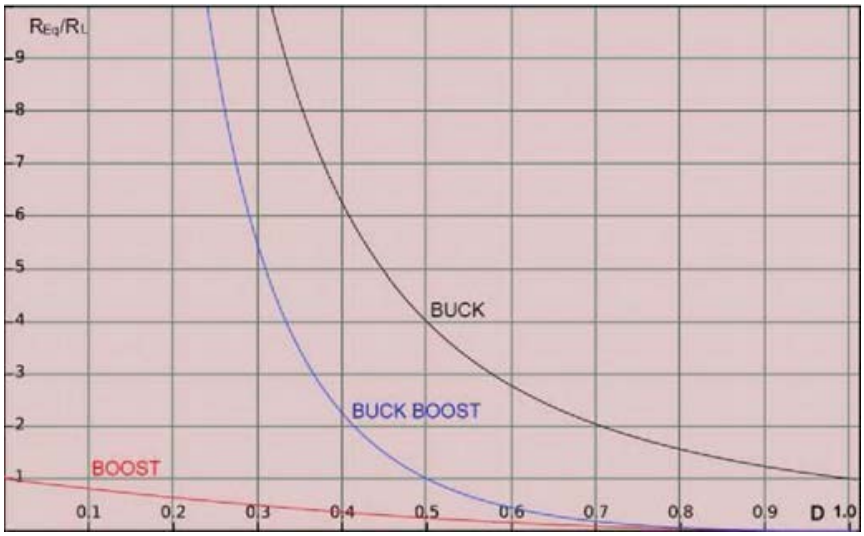

Figure 2.190 The dependency between R_{EQ}/R_R on duty cycle in DC-DC converters.

This function curve highlights how varying the duty cycle affects impedance matching between the fuel cell system and the load, ensuring optimal power transfer and stable operation of the drivetrain.

From the analysis, presented in [38], the following key conclusions are drawn:

- Duty cycle adjustment in the DC-DC converter controls the equivalent input impedance, allowing regulation of fuel cell voltage, current, and power.

- The type of DC-DC converter (buck, boost, or buck-boost) must be selected based on load requirements and energy storage constraints.
- The relationship between duty cycle and fuel cell input impedance is nonlinear.

To maintain optimal operation, a closed-loop control system (Figure 2.191) dynamically adjusts the equivalent input impedance. Since the fuel cell response is slow, impedance must be gradually modified when transitioning between operating points. However, sudden load changes require rapid impedance adjustments to stabilize output power.
A digital microprocessor-based controller is employed, converting analogue sensor data into digital signals for precise regulation. The input current of the DC-DC converter (fuel cell output current) serves as the control reference.

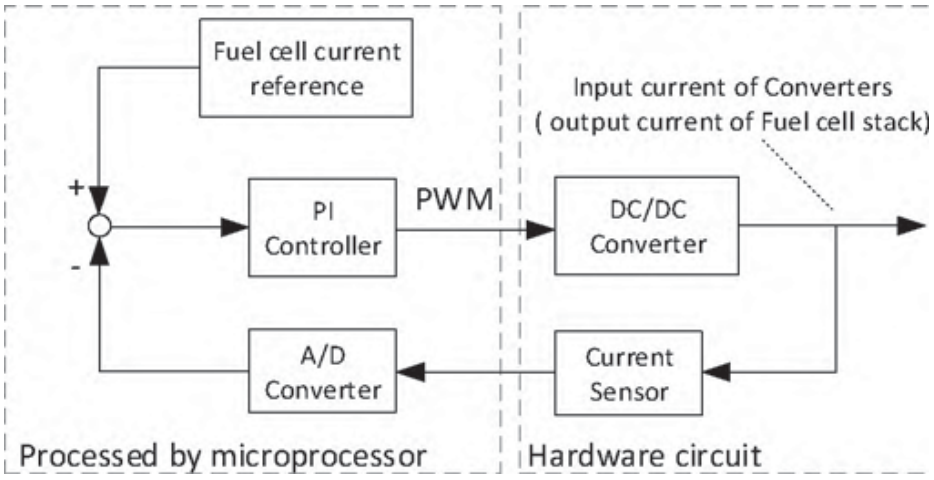

Figure 2.191 The control block diagram of the converter circuit.

Figure 2.192, illustrates continuous and discrete current references, where the internal microprocessor interrupt function generates stepwise adjustments. The incremental *PI* controller modifies the *PWM* signals, ensuring the fuel cell output current follows the reference value.

To prevent overloading, the *PWM* duty cycle is constrained, ensuring safe operation within fuel cell limits. The control circuit is integrated with the fuel cell management system, maintaining current reference values within safe operating ranges.

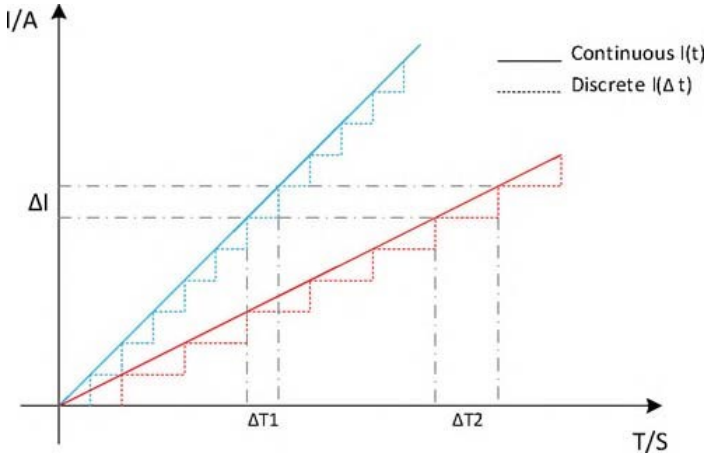

Figure 2.192 The current reference in continuous and discrete modes.

Implementation of fuel cell control strategy on a test platform

In Configuration II, the fuel cell output current gradually increases during start-up until the DC-DC converter reaches unity duty cycle, connecting the fuel cell to the *DC* bus in passive hybrid mode. During shutdown, the current gradually decreases to zero for a smooth transition.

To implement this control strategy, a test platform (Figure 2.193) was built. The system consists of a power supply simulating fuel cell output characteristic, a 2kW synchronous buck converter, a 50V, 300Ah lithium iron phosphate battery pack, and a 2.4kW electronic load for simulating load variations. A microprocessor (Arduino ATmega32U4) is used to manage *PWM* control, *PI* regulation, and system monitoring, while LabVIEW software facilitates real-time data acquisition (Figure 2.194).

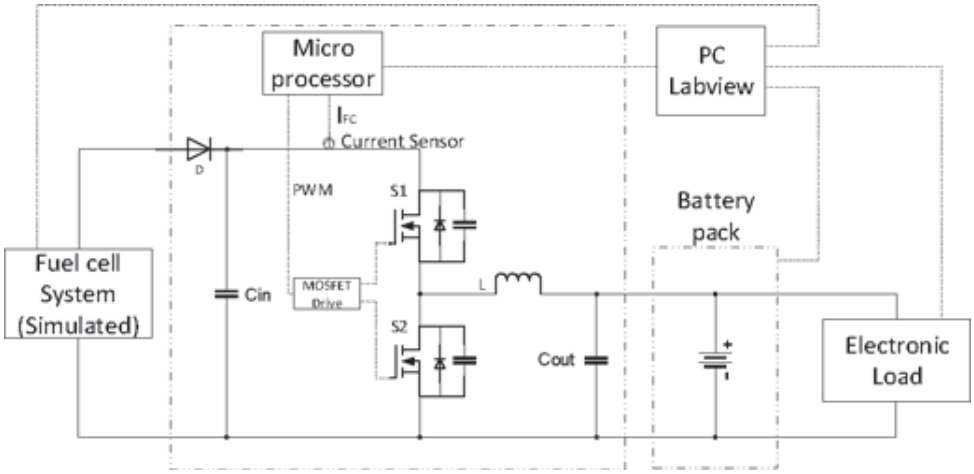

Figure 2.193 The schematic of the test platform.

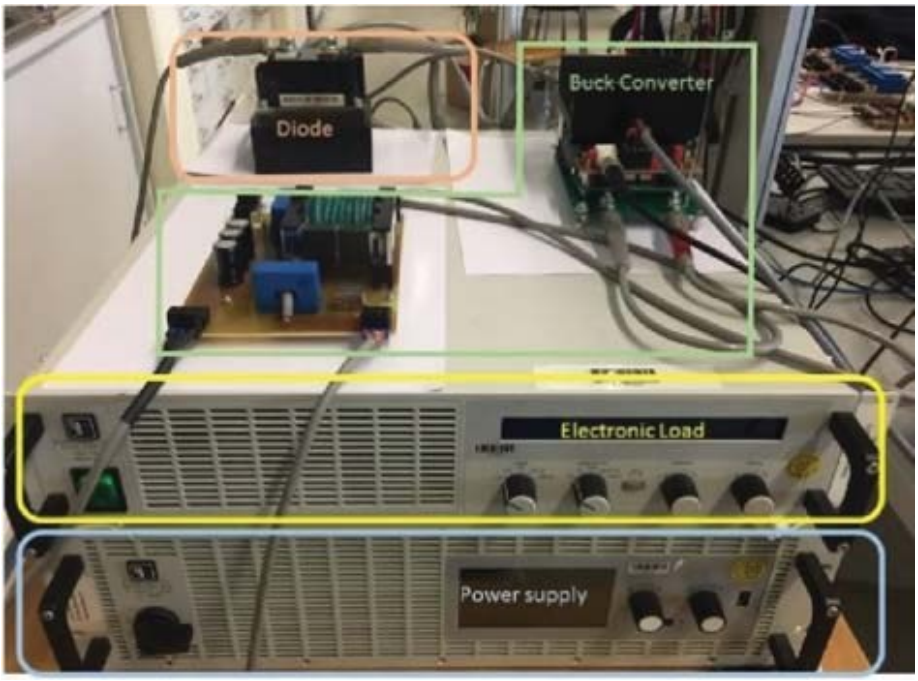

Figure 2.194 Test platform for control strategy realization.

Due to DC-DC converter power limitations, the simulated fuel cell system operates at a modulated output curve, as shown in Figure 2.195. It has an open circuit voltage of 80V, a nominal power of 2.3kW, and an operating voltage of 50V at 47A nominal current. The Arduino ATmega32U4 controls the PWM signals. A high precision 50A→5V current sensor is used. A custom adapter board integrates the power supply and the data interfaces, Figure 2.196.

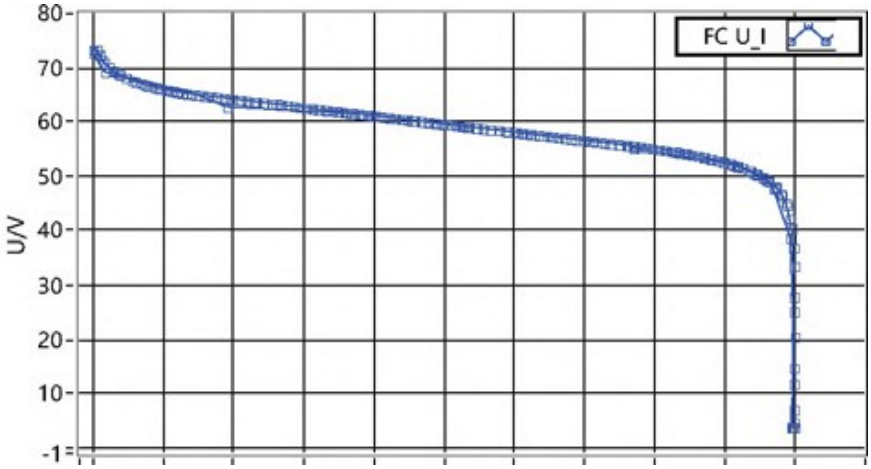

Figure 2.195 The output behaviour U-I curve of the simulated fuel cell system.

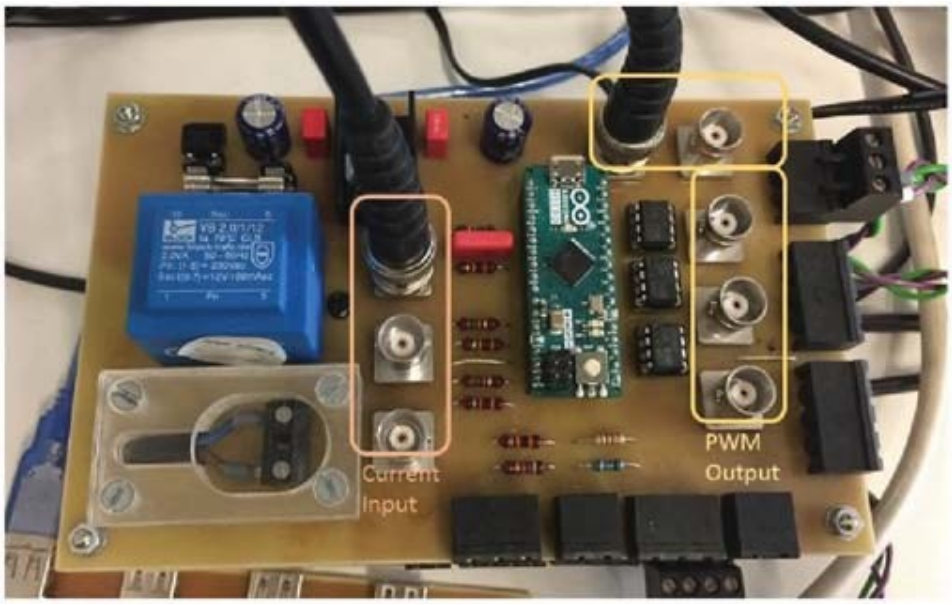

Figure 2.196 Control unit for the buck converter circuit.

The closed-loop control system follows the schematic in Figure 2.197. Initially, the interrupt period is set to match the required current rise rate. Once a start signal is received, the interrupt function generates a real-time current reference, and the *PI* controller adjusts the *PWM* signals. Interrupts update values continuously with minimal delay (Figure 2.192). When the termination condition is met, the *PI* controller and interrupt function deactivate, preparing for the next cycle.

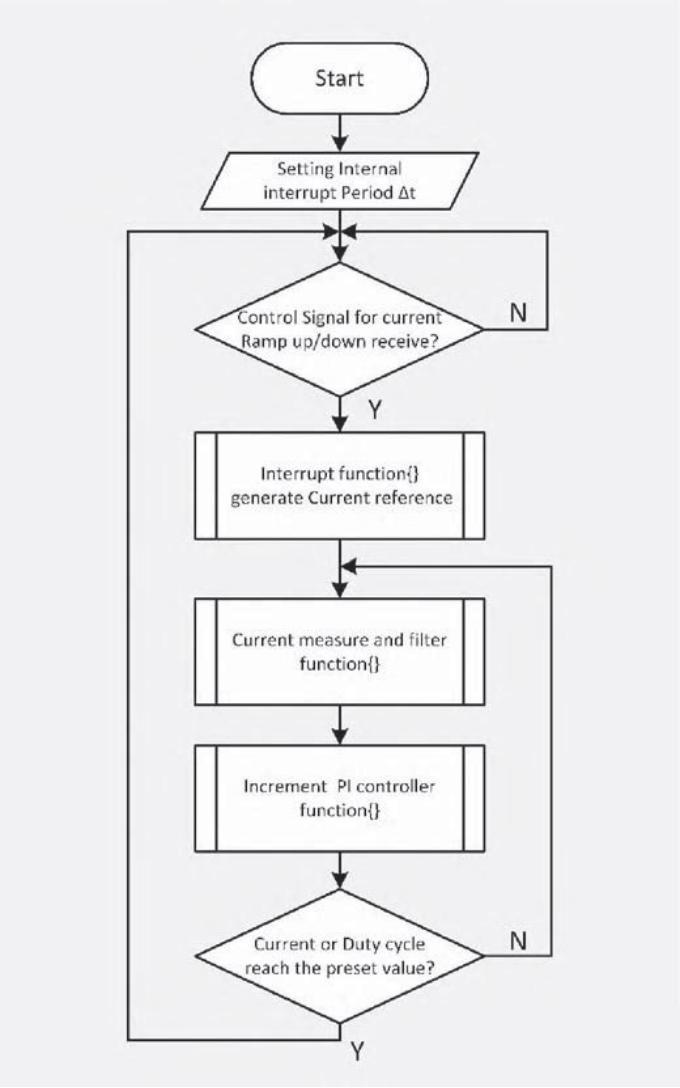

Figure 2.197 Control strategy flow diagram of the fuel cell system.

This adaptive strategy ensures smooth current transitions, preventing voltage spikes and stabilizing fuel cell operation in a passive hybrid system.

Practical measurements in the test platform

The experimental results of the proposed control strategy are shown in Figure 2.198-Figure 2.200. The fuel cell system outputs current (red line) ramps up and down at 4A/S (Figure 2.198), 2A/S (Figure 2.199), and 1A/S (Figure 2.200), increasing from 0A to 40A before gradually returning to 0A. The load current (blue line) fluctuates between 0A and 40A, while the battery current (green line) reflects charging and discharging behaviour. The horizontal axis represents time unit, with 200ms measurement intervals (50 → 10s).

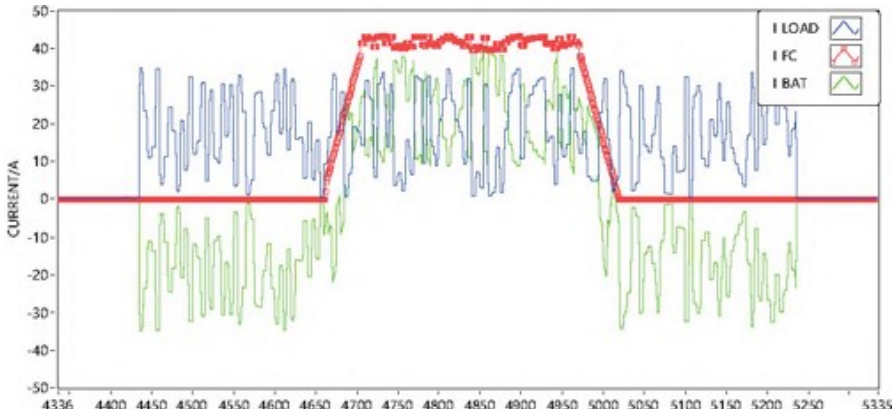

Figure 2.198 Response to fuel cell system current ramp up and down with 4A/S rate.

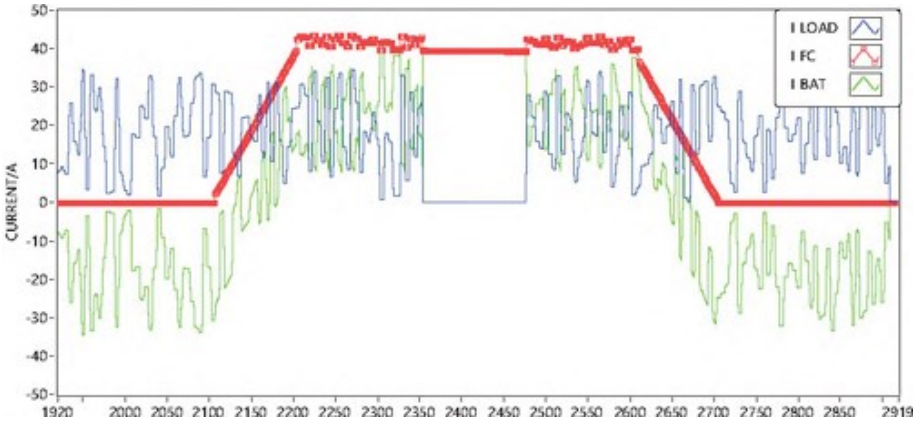

Figure 2.199 Response to fuel cell system current ramp up and down with 2A/S rate.

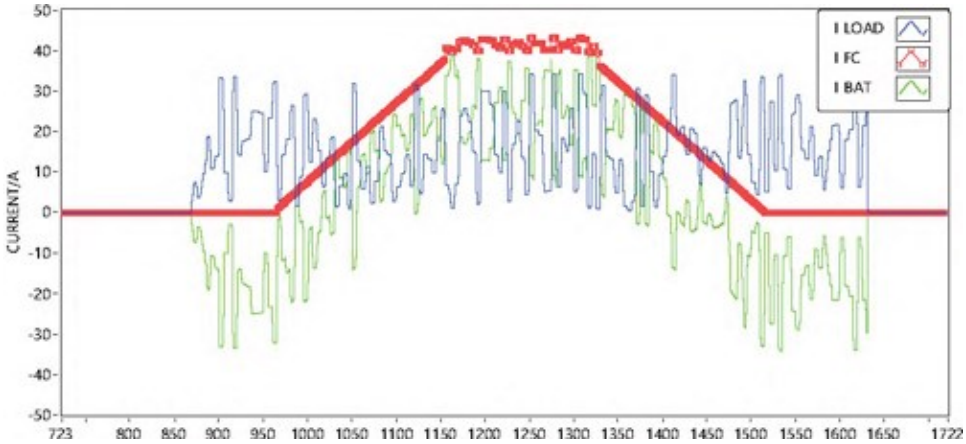

Figure 2.200 Response to fuel cell system current ramp up and down with 1A/S rate.

The proposed control method ensures smooth fuel cell power regulation while quickly responding to load variations. The current change rate remains stable, unaffected by load fluctuations, maintaining power stability.

Operating in passive hybrid mode, the fuel cell output current adjusts with DC bus voltage, minimizing DC-DC converter losses despite minor power fluctuations.

A small abrupt current change appears when the buck converter duty cycle reaches unity, due to PWM dead time in MOSFETs. However, this does not impact system stability, ensuring reliable performance.

2.2 Academic and professional activity

After obtaining my PhD degree on July 30, 2015, I have been actively engaged in academia, contributing to both teaching and research in the field of electronics.

In the fall of 2015, I began my academic career as an associate professor at Politehnica University of Timișoara (UPT), at the Faculty of Electronics, Telecommunications and Information Technologies (ETcTI), Applied Electronics Department. I contributed to the laboratory activities for the courses "Electronic Circuits and Devices " and "Electronic Circuits Fundamentals".

From February 2016 to February 2017, I acted in the position of teaching assistant in the Department of Applied Electronics, where I expanded my teaching classes to include also "Fundamentals of Electronic Engineering", "Analog Integrated Circuits" and "Power Electronics".

Between 2017 and 2020, I was in the position of lecturer, where I delivered both lecture and laboratory teaching activities. Notably, I conducted courses in "Fundamentals of Electronic Engineering" and "Materials, Components, and Electronic Technology". My laboratory teaching activities covered subjects such as "Fundamentals of Electronic Engineering", "Analog Integrated Circuits" "Electronic Circuits and Devices", "Electronic Circuits Fundamentals", "Electronic and Optical Devices" and "Power Electronics".

Since February 2017, I have been promoted to the position of associate professor, where I have taught courses in "Materials, Components, and Electronic Technology", "Fundamentals of Electronic Engineering" and "Electronic and Optical Devices" and from 2022, also the course "Analog Integrated Circuits". I expanded the teaching activities with a seminar for "Analog Integrated Circuits", and the laboratory and project activities for “Power supplies”. Note that the "Analog Integrated Circuits" is for the English bachelor program and "Power Electronics" for both, English and Romanian bachelor program.

For the current courses as well as for laboratory, seminar or project activities adequate teaching materials (books, laboratory guides, lecture notes, laboratory notes, problem collections, presentations, etc.) are available both physically and in electronic format on the Virtual Campus.

I have co-authored four specialized books entitled "Electronică de putere.Experimente", "Circuite electronice fundamentale. Teorie și probleme", "Electronic Circuits Fundamentals. Theory And Problems" and "Dc-Dc Converters-Analysis, Design, Experiments". These books serve as useful resources for the students, supporting their coursework, laboratory, and seminar activities, as well as for professionals in the respective fields.

In my teaching approach, I have integrated modern teaching methods such as interactive presentations and discussions, problem or project-based learning, simulations and collaborative learning. Additionally, I have incorporated interactive online tests and educational hackathons to enhance student engagement. For laboratory activities, we employ both hands-on experiments and simulation-based analytical methods to provide a comprehensive learning experience.

Course syllabuses have been designed, adapted and regularly updated to comply with current international academic standards and industry requirements, ensuring that students acquire relevant and up-to-date knowledge and skills.

The rapid evolution of the electronics and telecommunications field forces the need for continuous updates in engineering education. Throughout my academic career, I have been dedicated to modernize and enhance the curriculum, ensuring that the content delivered to the students remains updated with the technological advancements and industry expectations. For example, I have integrated modern semiconductor materials, including Silicon Carbide (SiC) and Gallium Arsenide

(GaAs) into the curriculum, enriching students' understanding of advanced electronics. Another example can be observed in the Materials for Electronics (MPE) course, taught in the first year, first semester. As the first electronic engineering discipline that first-year students encounter, it plays a crucial role in sparking their interest in the field. To enhance engagement and deepen their understanding, I collaborated with Associate Professor Dr. Eng. Adrian Popovici, who also teaches this course, and Assistant Ph.D. Candidate Eng. Cristian Ionici to develop and implement new laboratory topics starting from the 2023–2024 academic year. The MPE course explores various classes of materials, components and their applications in electronics. The course now includes essential characteristics and relevant applications of sensors, providing students with a modern perspective on the current and future uses of these devices in engineering. This approach not only ensures the continuous modernization of course content but also enhances the course attractiveness by aligning it with industry trends, thereby better preparing students for the challenges of contemporary electronics engineering.

As part of the project, for the “Power Electronics” course, students are required to design a converter from some specifications. They follow identical methodology to that applied in the industry, which includes conducting a theoretical analysis, simulating the converter, comparing the theoretical analysis with the simulation results, and ultimately implementing a practical prototype. In addition to working with state-of-the-art semiconductor devices, students also have the opportunity to be familiar with dedicated integrated circuits for controlling DC-DC converters. For the theoretical analysis of power structures, I guided students in installing and using specialized software tools that enhance their analytical and design capabilities. Specifically, *MATLAB* is employed for assisted design, *CASPOC* is used for simulations, and *Visio* or *Diagram Designer* are recommended for schematic design and waveform plotting. By integrating these tools into their workflow, students gain practical experience with industry-relevant software, allowing them to develop a structured and systematic approach to power electronics design. This methodology not only strengthens their theoretical understanding but also enhances their ability to visualize, simulate, and optimize complex electronic systems.

This comprehensive approach ensures that they gain both theoretical knowledge and practical experience, preparing them for real-world engineering challenges.

In the Analog Integrated Circuits course, in addition to using the Orcad-Spice simulation environment, I have incorporated the use of dedicated development boards from Texas Instruments.

Incorporating innovative methods to enhance both the attractiveness and efficiency of learning is a key aspect of my teaching approach. For example, in the courses “Electronic Circuits Fundamentals” and “Electronic Circuits and Devices”, students have access to simulations using upgraded open-source software packages such as LTSpice, while for circuit design and analysis, *Electronic WorkBench* is employed. These programs are installed on the laboratory computers and are also available for students for use on their personal devices due to their open-source nature. This approach enables students to compare simulation results with experimental data, fostering deeper learning and a more comprehensive understanding of electronic concepts. By integrating simulation tools into coursework, students develop essential analytical skills and gain hands-on experience.

How it can be seen, I have prioritized the integration of new methodologies, modern software tools, and practical applications to ensure that students receive a comprehensive, well-structured, and industry-relevant education. This commitment is reflected in my efforts to regularly

update course materials and laboratory activities, maintaining a dynamic and engaging learning environment.

A crucial part of my academic contributions has been the modernization and expansion of laboratory infrastructure to support practical learning and hands-on experimentation. One of my most impactful projects has been the expansion of the “Electronic Circuits and Devices” and “Electronic Circuits Fundamentals” laboratory, which share the same room, and I consider that they are an essential component for bachelor students. Collaborating with my colleagues Radu Mirsu and Aurel Filip, and also with the support of the bachelor student Daniel Marpozan, from sponsorship, we managed to change and increase the number of fully equipped workstations to eight. Each workstation was fitted with a dual-channel power supply, a digital oscilloscope, a function generator, a multimeter, and a dedicated computer. This enhancement significantly improved student engagement and provided greater access to high-quality instrumentation for hands-on experimentation. Further supporting the development of hands-on experience, I worked alongside with a group of students to assemble and populate printed circuit boards, which are now actively used in the laboratory experiments.

In addition to my work on” Electronic Circuit and Devices” laboratory, I have also contributed to the enhancement of the “Power Electronics” laboratory, ensuring that students and researchers have access to cutting-edge experimental tools. This was made possible through national research grants I won, allowing for the acquisition of advanced laboratory equipment.

Collaborations with Analog Devices company resulted in equipping the “Electronic Device” and “Power Electronics” laboratory with eight units each of ADALM2000, ADALM2000 BNC Adapter Board, and ADALM2000 Power Booster Board, provided by the company.

Coilcraft company contributed to the enhancement of “Power Electronics” lab, by supplying state-of-the-art inductors. These components are essential for both the practical implementation of educational projects, either in laboratory coursework or diploma projects and for advanced research applications.

I have actively contributed to the continuous development of undergraduate study programs, including Applied Electronics (EA) field and Technologies and Telecommunications Systems (TST English). Additionally, I participated in the introduction and implementation of a new undergraduate program: Microelectronics, Optoelectronics, and Nanotechnologies (MON). For all these study programs, overseen by the Department of Applied Electronics, I was involved in the preparation of accreditation documentation. More than that, for the TST English program, together with Prof. Dan Lascu and Prof. Aurel Gontean, I was directly responsible for the accreditation documents.

Furthermore, I am currently leading efforts with my colleagues Bogdan Marinca, Georgiana Simion, Elisei Ilies, and Magda Marinca for the authorization of the new MON bachelor program.

Beyond research and teaching, I supervised undergraduate and master's thesis projects, the majority of which have had practical applications.

Between 2016 and 2025, I supervised 87 students in total, in their bachelor diploma and dissertation projects, providing them with academic and practical support. Among them, 66 students completed their diploma projects, and 10 of these projects were developed in collaboration with industry partners. Additionally, I guided 21 dissertation students, out of which 7 theses were conducted in direct partnership with companies, strengthening the link between academia and industry.

My involvement in research further extended, as I mentored more than 20 master's students in research studies, allowing them to engage in deeper technical exploration within electronics and telecommunications. Four students are continuing their studies with PhD. They are enrolled like PhD students, at prof. dr. Eng. Dan Lascu, and we are continuing our collaborations.

I have consistently and constantly encouraged students to participate in electronics competition, in research teams and to present their work at scientific communication sessions, including both student symposia and international conferences. In 2023, Medinceanu Paul, in "Tudor Tanasescu", national conquest on "Analog Integrated Circuits", where he was trained by the undersigned, Bogdan Marinca and Mircea Gurbina, won the third place. I collaborated with 10 students on research projects, resulting in the publication of 19 papers indexed in ISI (WoS) or IEEE. Furthermore, I helped with the integration of students into the "Power Electronics" research group, thereby supporting their professional and academic development through hands-on involvement in ongoing research activities.

Through a partnership between UPT and the "Babel" School, in 2022, I have actively contributed to STEM education at a younger level, organizing and supporting two laboratories on electronic and optoelectronic devices for 6th-grade pupils. This initiative aimed to spark curiosity and develop an early interest in electronics and engineering among young learners.

Since 2022, each summer I have taught a course and I have conducted six laboratory sessions at the Electronics Summer University (ESU), organized by LSFETC (ETC Students League), for high school students in the 11th and 12th grades. These sessions provide a hands-on learning experience, combining theoretical principles with practical applications to enhance students' understanding and increase their interest in electronics.

My dedication to educational excellence and student mentorship has been formally recognized through the yearly "Ioan de Sabata" Prize for Excellence in Education, which I have been honoured to receive three consecutive years. This prestigious award acknowledges my commitment to high-quality teaching, curriculum development and student success, further reinforcing my role in shaping the next generation of engineers and researchers.

My commitment to international academic collaboration is reflected in my recurring role as an invited lecturer through the Erasmus program at Jade University in Germany. I also participated as a visiting professor at the University of Angers in France. The collaboration with Jade University has led to joint student projects, including a PhD project supervised from Jade University by Dr. Eng. Folker Renken and co-supervised at UPT by Professor Dr. Eng. Dan Lascu.

Regarding lifelong learning and professional development, I continually enhanced my skills by attending advanced courses in my field. One of my recent professional development endeavours includes specialized course on "Introduction to Analog IC Design, Simulation, Layout, and Verification, in-person training using Synopsys Custom Compiler tool flow, STFC," held in Didcot, Oxfordshire, UK, from March 12 to March 14, 2024. Additionally, I have attended training sessions offered by IEEE Continuing Education, specifically "Modelling and Simulation of MEMS Devices" and "Modelling Eddy Current Inductive Sensors in COMSOL". These courses allow me to stay at the forefront of technological advancements and bring the latest knowledge into my academic and research activities.

The Flex Company, donated to our faculty a surface mount technology (SMT) production line. This state-of-the-art facility, valued at €250000, the highest donation in UPT ever received at once from a company, is located in the SPM building and is now being used in labs, student practice sessions, and diploma projects. In this regard, I participated in the training sessions organized by Flex Company, focused on the use of the SMT production line. The training, spanned for two weeks and covered various production lines and provided insights into modern electronics manufacturing techniques.

In December 2022-2023, we hosted Flavio Sestagalli and Vittoria Greco, representatives from Coilcraft company, who conducted three specialized lectures on power inductor design. These specialized courses have provided valuable insights and practical experience with state-of-the-art tools and methodologies, allowing me to integrate the latest industry-relevant knowledge into both my research activities and my teaching practices.

Throughout my academic career, I have been actively involved in managerial and research-related responsibilities that contributed to the educational process and institutional development.

Managerial and Research Activities in the Educational Process

- I have contributed to university promotion through participation in VIP EDU, the development of promoting materials for undergraduate programs, and involvement in VisitUPT, a 3D virtual fair for prospective students.
- I actively participated in the Open Campus Night, part of the European Researchers' Night 2023, organized by UPT. Representing the Department of Applied Electronics (EA), other participants included Prof. Dr. Eng. Dan Lascu, Assistant Eng. Phys. Septimiu Lica, as well as students Paul Bodea, Bogdan Preda, and Mihai Popescu.
- I have been engaged in the admission committee for ETcTI and/or Automation and Computing (AC) faculties.
- I have served as a tutor for first-year students since 2020.
- I hold the position of Head of the Student Counselling Office within the Faculty of Electronics, Telecommunications, and Information Technologies (ETcTI).
- Through my responsibilities is also included the participation in the diploma defence commission, where I assess and evaluate students' final projects.
- Regarding the doctoral research, I have served as a PhD guiding committee member for several doctoral candidates, including Corina-Nicoleta Covaci (Vidoni), Sorin Popescu, Ilieș Elisei, Marinca Magdalena, Delia Boțilă, Gabriela Jude, and Shen Wensong. Among them, two candidates have successfully defended their theses and obtained their PhD degree.
- I am a member in the Faculty Council and in the Applied Electronics Department Council, where I contributed to decision-making processes related to academic policies and curriculum development.
- I was a member in the organizing committee for academic events, including ISETC 2020, ISETC 2022, ISETC 2024 and OPTIM 2025 conferences
- I contributed as a chair and co-chair at prestigious international conferences, such as the Power Electronics and Motion Control Conference (PEMC) 2018 and 2020 edition
- Reviewer Board Member of MDPI Energies Journal
- Reviewer for:
    - MDPI Energies Journal

- IEEE Vehicular Technology Magazine
- ELSEVIER Energy Reports Journal
- MDPI Applied Sciences Journal
- MDPI Algorithms Journal
- MDPI Electronics Journal
- MDPI Sensors Journal
- MDPI Actuators Journal
- MDPI World Electric Vehicle Journal
- EPE Conference
- PEMC Conference
- ISETC Conference

- Additionally, I am an active member of several professional associations, including:
  - IEEE Industry Applications Society
  - IEEE Power Electronics Society
  - IEEE Industrial Electronics Society
  - Electronic Engineers Association, Timișoara

- I was responsible for 2 grants, valued at minimum 10000$:
  - "Proiecte de Cercetare - Dezvoltare pentru tineri cercetători PCD-TC-2017, "Convertoare multifază pentru conversia energiei solare şi încărcarea acumulatorilor din vehiculele electrice", Nr. 33"
  - "Unitatea Executiva pentru Finantarea Invatamantului Superior, a Cercetarii, Dezvoltarii si Inovarii (UEFISCDI) Programul 1 – Dezvoltarea sistemului național de cercetare-dezvoltare Subprogramul 1.1 – Resurse umane/Proiecte de Cercetare Postdoctorală, PN-III-P1-1.1-PD-2019, "Noi familii de convertoare dc-dc în comutație de tip hibrid cu aplicații în sisteme de încărcare a bateriilor din vehicule electrice și în conversia energiei solare""

- Member in 3 grants, valued at minimum 10000$:
  - Granturi Naționale de Cercetare - ARUT 2018, "Soluții embedded pentru implementarea structurilor neuronale profunde (Deep Neural Networks)", ID 132
  - 123900-Asigură-ți Viitorul prin Educație și Antreprenoriat - AVEA, Contract de finanţare nr. POCU/379/6/21/123900
  - PolitehnicaNouluiSecol: platformă online pentru sporirea accesului tinerilor la învățământul superior și reușita pe piața muncii SmartUPT
- 41 papers indexed WoS (formerly ISI), from which:
  - 9 WoS Journal (8 of them Q1 and Q2)
  - 32 WoS Conference
- 12 BDI papers

My career as an academic staff member, researcher, and mentor is driven by my commitment to academic excellence, student success, and industry collaboration. By fostering a dynamic learning environment, engaging in impactful research, and establishing strong partnerships with leading industry partners, I aim to provide students with the knowledge, skills, and opportunities needed to thrive in their careers. My efforts are centered on advanced education, promoting innovation, and ensuring that students graduate with both theoretical expertise and practical

experience, enabling them to make meaningful contributions to the field of electronics and telecommunications. Through continuous improvement, mentorship, and engagement with industry, I remain dedicated to educate and teach the next generation of engineers, researchers, and innovators who will drive technological progress and shape the future of electronic systems.

A fundamental aspect of my professional career is my continuous commitment to learning and updating my knowledge, ensuring that I remain connected to technological advancements and developments in the field.

3. Future academic, professional and research activities

The scientific, professional and academic activities of academic teaching staff are highly interconnected and mutually supportive, playing an essential role in their continuous development. However, each of these areas has its own specific characteristics and requirements, making it necessary not only to maintain a balance between them but also to continuously optimize each activity individually. A balanced and efficient approach, aimed at enhancing both individual performance and the quality of education and research, is essential to ensuring constant and sustainable progress in the academic environment.

The context in which I plan to build my future academic career is structured into three main directions: academic, professional, and scientific activity, and is based on a set of values: feedback, transparency, openness to innovation, and community. I rely on the support for these values from the staff of the Applied Electronics Department of Politehnica University Timișoara, the higher education institution where I work, which is part of the group of highly trusted advanced research and education universities in Romania, and on their further promotion among collaborators. I believe that the development of the electronics field and related disciplines, as well as my professional growth together with that my colleagues, are dependent on respecting and maintaining these values.

Continuous feedback serves both as a means of personal evaluation and as a mechanism for assessing the work of others, forming the foundation for ongoing improvement. The establishment of a strong academic community and the development of effective professional relationships rely on the exchange and integration of feedback. I am committed to fostering and utilizing feedback in all areas and my professional activity, whether in teaching (through student evaluations), in scientific research (via review sessions and internal presentations), and in professional development (through open discussions and consultancy).

The transparency of information and decision-making processes are essential for building open, engaged, and collaborative teams, groups, and communities. My experience within the teams I have worked with has shown me that transparency plays a fundamental role in their effective operations, facilitating clear and efficient communication among members. Beyond its obvious benefits, transparency fosters a relaxed working environment where all team members are well-informed and actively involved in decision-making. Additionally, any concerns can be openly expressed and turned into constructive feedback, contributing to continuous improvement.

In a highly dynamic field such as electronics, openness to innovation is not merely an option but a necessity for any professional. Emerging technologies must be embraced and assessed as soon as they appear to remain competitive and innovative. In the academic environment, where there is less pressure for immediate product releases compared to the industry sector, this openness becomes a significant advantage, allowing innovative solutions to be explored without financial constraints. I have always been and intend to remain curious, enthusiastic, and eager to acquire knowledge, always on the lookout for future breakthroughs, and developing innovative solutions to persistent challenges—keeping an open mind and maintaining my enthusiasm at the highest level.

3.1 Future academic and professional activity

The career of an academic teaching staff member inherently involves a continuous process of personal and professional development, essential for providing students with a broad, up-to-date, and relevant perspective on the field taught. Regardless of his/her specialization, a teacher in the university must always stay informed about the latest discoveries, technologies, and methodologies in his area of expertise, with the responsibility of integrating this knowledge into both the educational and research processes. In this regard, I aim to actively participate in prestigious international conferences in the field of "Power Electronics" by publishing scientific papers that I hope to contribute to the advancement of knowledge in this domain. Additionally, an important objective is to publish at least one paper per year in internationally indexed WoS scientific journals, preferably in publications with a significant impact factor, to increase personal and university visibility and recognition within the global scientific community.

Another fundamental aspect of my academic activity is supporting and encouraging students to engage in research activities by participating in conferences, symposia, and competitions at both national and international levels. I strongly believe that stimulating students involvement in such activities provides them with the opportunity to develop critical thinking, creativity, and the ability to apply theoretical knowledge in practical contexts.

As an academic teaching staff, I have the responsibility to guide and stimulate students' natural curiosity and spontaneous interest in discovery. It is essential to mentor and support them in organizing and integrating the knowledge they acquire such that they can apply it to solve real-world problems. At the same time, I consider crucial to offer them the freedom to examine and critically analyse information, to cultivate their independence in work, and to impose a sense of responsibility for their actions. This approach not only enhances their academic and professional skills but also prepares them for the challenges of a dynamic and competitive work environment. Through these initiatives, I aim to contribute to improving the quality of education in the field of electronic engineering and to promote excellence both in teaching and research, thus strengthening the university environment as a space for innovation, collaboration, and progress.

For all the subjects in which I will conduct teaching activities, I will ensure the availability of comprehensive and high-quality study materials in both physical and electronic formats on the Virtual Campus platform. These teaching materials will be continuously refined and updated to align with the latest educational standards and the evolving requirements of the labour market. By keeping these materials updated, I will guarantee that students will have access to the most relevant and up-to-date academic content, fostering a learning environment that is both dynamic and responsive to industry advancements.

According to the principle of "student - centered learning," I will implement modern teaching and assessment methods, including interactive presentations, applied discussions, and multiple-choice evaluations, designed to enhance student engagement and understanding. In laboratory activities, I will apply advanced analysis methods based on simulation and practical experiments. Additionally, I will expand this laboratory gained experience and experiments into digital formats via the e-laboratory concept, which will allow students to gain practical knowledge through an immersive, technology-driven approach. Moreover, I will promote the adoption of cutting-edge technological tools that encourage active participation, collaboration, and innovative problem-solving among students.

To accomplish these objectives, it will be essential to maintain continuous professional development through the consistent updating of both specialized subject knowledge and pedagogical techniques. In pursuit of this goal, I will participate in technical conferences,

education dedicated conferences, professional workshops, and exchange programs with partner universities, both nationally and internationally, facilitated through Erasmus+ and EUDRES mobility programs. These valuable experiences will significantly contribute to the development of my teaching methods, enabling the integration of globally recognized best practices into my educational activities. Furthermore, they will contribute to strengthening professional networks and fostering collaborations that enhance the overall quality of instruction.

Another significant focus will be on improving the laboratory infrastructure, ensuring they are equipped to support both advanced research and high-quality teaching activities. To achieve this, I will explore various funding opportunities and participate in academic competitions that offer access to state-of-the-art equipment and innovative technological solutions. By participating in competitions and accessing available funding through national and international research grants and projects, I will contribute to the development of a modern educational environment capable of meeting current demands in the field of engineering. One notable project contributing to this goal is the Important Projects of Common European Interest (IPCEI), in which UPT will serve as an indirect partner, alongside leading industry players NXP and Continental.

Furthermore, together with Prof. Dr. Eng. Dan Lascu and Prof. Dr. Eng. Mihaela Lascu, I am responsible for the Power Electronics and Sensors Lab. This collaboration and participation in the IPCEI project will enable us to acquire cutting-edge equipment such as electronic loads, power supplies, data acquisition boards, NI CompactRIO systems, frequency response analyzers, Ridley Boxes, mixed-signal oscilloscopes with current probes, and signal generators. Moreover, conceiving new integrated circuits for switching converter controls will be a challenging task. By leveraging available funding through national and international research grants and collaborative projects, we will significantly contribute to the development of a modern educational environment capable of meeting the current and future demands in the field of electronic engineering.

Having accumulated a decade of experience in academia and research, during which I have guided numerous bachelor and master students in their graduated thesis and research internships, I will continue to engage students in meaningful and practical research initiatives. Encouraging their participation in active research groups will be a priority, as it not only cultivates academic excellence but also fosters the development of essential analytical and problem-solving skills. A long-term aspiration of mine will be to extend my mentoring role in supervising doctoral students, thereby playing an integral part in shaping the next generation of specialists.

Each year, a number of highly accomplished master graduates expressed their desire to continue their doctoral studies in the field of electronics, telecommunications, and information technologies. By creating a dynamic and intellectually stimulating research environment and providing a well-structured academic trajectory from bachelor to doctorate levels, I intend to contribute to the development of highly competent professionals, capable of addressing current and future technological challenges that arise in the industry.

3.2 Future research activity

Future research activities will align with current scientific challenges, market demands, existing competencies, and available technical capabilities. A careful balance between fundamental and applied research will be maintained to ensure that the outcomes meaningfully contribute to both scientific advancement, technological and industrial innovation.

The experience gained in supervising bachelor and dissertation projects, master research activity, in participating in PhD advisory committees, as a member or conducting the teams in the

research grants and in writing papers represents a considerable advantage in planning, guiding and monitoring the research activities of future PhD students. The development plan for supervising PhD students involves several fundamental aspects, including guiding them on conducting scientific research in accordance to ethical principles and providing continuous guidance and support throughout their research stage, from the initial planning phase to the completion of their PhD thesis. Adequate infrastructure to meet the specific research objectives will be provided, alongside with stimulating their active involvement in research projects pertinent to their area of study and competence.

The primary research direction, where also the PhD students can be engaged, will focus on the development of advanced power electronic converters used in DC grids by exploring new control methods for DC-DC converters and the integration of artificial intelligence-based technologies (AI) in power electronics. The implementation of these technologies is expected to open new research directions, with direct applicability in design optimization, control strategy improvement, and enhance the reliability and efficiency of the conversion systems.

In the optimization of converter design, artificial intelligence algorithms will be employed to refine the design parameters of power electronic converters, facilitating improved performance and reducing the development time. Advanced modelling and simulation techniques will play a crucial role in expediting these developments. Additionally, the implementation of sophisticated control strategies will be pursued by incorporating AI-driven methods such as reinforcement learning to enhance converter performance under diverse operating conditions. The adaptability and robustness of these systems will be further improved through the development of adaptive control algorithms.

Fault diagnosis and prognosis will also constitute a significant research area, with machine learning and deep learning techniques being deployed for early fault detection in power electronic systems. The integration of predictive maintenance strategies will contribute to increased system reliability and longevity. Moreover, advancements in energy management will be explored by optimizing energy consumption and storage within DC networks through AI-based approaches. The development of intelligent algorithms will enhance the efficiency of energy distribution and utilization, furthering the sustainability and resilience of power systems.

The integration of artificial intelligence will extend to sustainable practices throughout the lifecycle of power electronics products, from material selection to recycling and reuse. AI-driven innovations will also be instrumental in control and thermal management, where predictive modelling techniques will be applied to optimize heat dissipation and enhance the longevity and operational efficiency of power electronic devices.

In this context, the research direction represents an excellent opportunity for PhD students to engage in cutting-edge scientific inquiry, while benefiting from a structured and supportive supervising plan.

Given the financial constraints associated with research activities, participation in competitive funding opportunities at both national and international levels will be essential for securing the resources necessary to sustain these efforts. This challenge also presents an opportunity to foster interdisciplinary collaboration and establish strategic partnerships with academic and industrial institutions. The successful realization of these research objectives will rely on continuous and effective collaboration among experts from complementary fields, ensuring that technological innovations are rapidly integrated into practical applications. By developing a strong interdisciplinary research framework, the implementation of cutting-edge solutions in power electronics and smart energy systems will be facilitated, contributing to meaningful advancements

in the field and providing PhD students with a robust, supportive, and dynamic environment to highly perform in pioneering power electronics research and smart energy systems.
Encouraging PhD students to participate in national and international scientific events will be a priority, aiming to widely disseminate their research results. Financial support for conducting research internships, both nationally and internationally, will be facilitated mainly through research projects funds and then by internal sources. Joint supervision doctoral programs in collaboration with prestigious international universities will be actively encouraged and supported, promoting excellence and facilitating valuable knowledge exchange with highly rank scientific communities.

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Annexes

Annex 1 - List of figures

Annex 2 - List of tables