FLoating point Arithmetic units for Graphical applications in FPGAs

Goal of the project:
This project proposes to develop dedicated floating point architectures on FPGAs to suit the growing demand of graphic application on these platforms.

Short description of the project:
Recent studies indicate that FPGAs provide better watts/flops performance compared to graphical processing units (GPUs). Adding features such as flexibility and high degree of parallelism makes suitable candidates for implementing graphical accelerators on future embedded systems. The major novelty of the proposal consists in the design of high performance FP units using an efficient exploitation of the FPGA arithmetic resources, such as the embedded multipliers or block RAM modules. Thus, dedicated arithmetic units for reconfigurable devices will be provided. Two types of FP operations are targeted: multiply and multiply-accumulate architectures (used for matrix products, vector and matrix products and dot products) and combined division and square roots (used for matrix inversions, Euclidean distance computations, etc). These units will be the backbone of dedicated hardware accelerators (for vertex, geometry and pixel shader operations) for these types of applications.

Project implemented by:
University Politehnica of Timisoara, Computer Engineering Department

Implementation period:
October 2011 - October 2014

Aplicability and transferability of the results:
A major goal of the research is represented by providing adequate floating point support for Open Hardware initiatives. We intend to add high performance floating point functionality to open source graphics accelerators, such as the one provided for OpenRISC based platforms.

Main activities:
1. Development of FP multiply and MAF architectures for FPGA. FP multiply and MAF operations are especially important in multiplications between vector and matrices.
2. Development of FP combined division and square root for FPGA.
3. Development of hardware accelerators for graphic operations and applications implementation based on designed hardware.

Results: We have provided floating point units for very high radix division and square root. These units have the smallest DSP count for multiplication based division/square root methods. On the other hand, we have researched floating point units for multiplication and multiply-add fused operations. We have provided a hybrid integer-floating point multiplier and a high performance floating point multiply-add fused which relies on architectures of the DSP blocks in modern FPGAs. Our research has resulted in one ISI rated journal paper and four published or accepted conferences.

Research centre: Research Centre for Computers and Information Technology.

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"People who are really serious about software should make their own hardware."
Alan Kay